

COMPAL CONFIDENTIAL

MODEL NAME :EDC41
PCB NO :LA-G891P
BOM P/N :XXXXX

14 WHL-U UMA(non TBT)

Whiskey Lake U42


2019-02-12

REV : 1.0 (A00)

- @ : Nopop Component
- EMI@ : EMI Component
- @EMI@ : EMI Nopop Component
- ESD@ : ESDComponent
- @ESD@ : ESD Nopop Component
- RF@ : RF Component
- @RF@ : RF Nopop Component
- CONN@ : Connector Component
- DS3@ : Deep sleep support
- NDS3@ : non Deep sleep support
- CXDP@ : XDP Component
- RTD3@ : RTD Component
- NRTD3@ : RTD Component
- ST33@ : ST TPM Component
- 750@ : NUVOTON TPM Component

MB PCB	
Part Number	Description
DA8001GT000	PCB 2FB LA-G891P REV0 MB UU NAR 1

Layout Dell logo




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REV:X00
PWB:

Power CKT : *NORTHBAY 14UU_WHL_PWR_0128
GPIO map : X10_CSLP GPIO map Rev1.3_20180529

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Title

Cover Sheet

Size

Document Number

Rev

0.3

Date

Monday, February 25, 2019

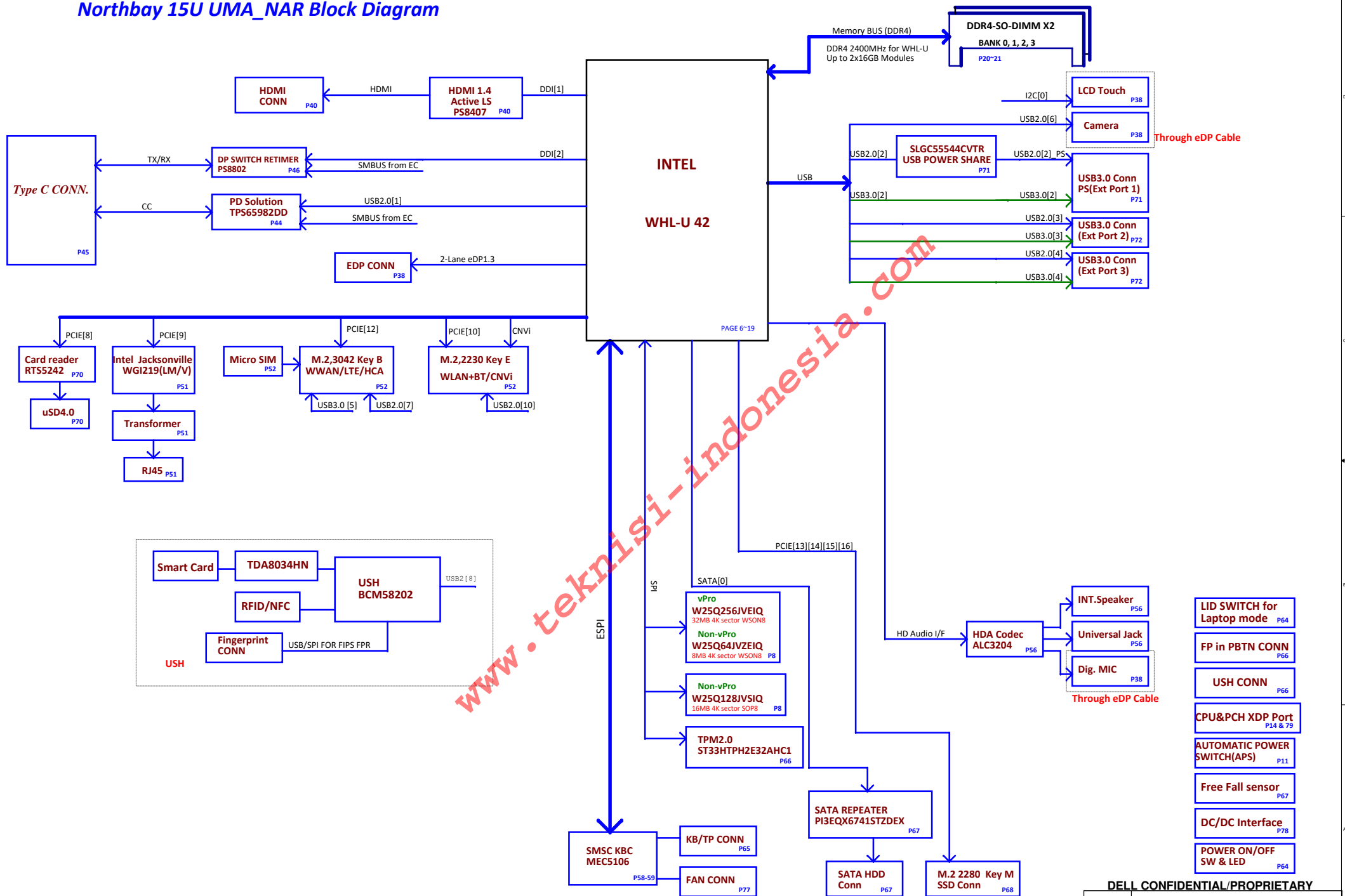
Sheet

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Northbay 15U UMA_NAR Block Diagram



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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S0ix/Moff	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S0ix (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

USB3.0	GbE	PCIE	SATA	DESTINATION
USB3.0-1		PCIE-1		Type-C
USB3.0-2		PCIE-2		JUSB1
USB3.0-3		PCIE-3		JUSB2
USB3.0-4		PCIE-4		JUSB3
USB3.0-5		PCIE-5		M.2 3042(LTE)
USB3.0-6		PCIE-6		NA
		PCIE-7		
		PCIE-8		Card Reader
		PCIE-9		LOM
		PCIE-10		M.2 2230(WLAN)
		PCIE-11	SATA-0	HDD
		PCIE-12	SATA-1	M.2 3042(LTE)
		PCIE-13		
		PCIE-14		
		PCIE-15	SATA-1*	M.2 2280 SSD (PCIex4 or SATA)
		PCIE-16	SATA-2	

USB PORT#	DESTINATION
1	Type-C
2	JUSB1
3	JUSB2
4	JUSB3
5	NA
6	Camera
7	M2 3042(WWAN)
8	USH
9	FPR in PB
10	M.2 2230(BT)

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1V_PRIM	+3.3V_CV2 +1.2V_MEM +2.5V_MEM	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +1.2V_RUN
S0	ON	ON	ON
S0ix	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 # 1	USB3.1 Gen1/Gen2 # 2	USB3.1 Gen1/Gen2 # 3	USB3.1 Gen1/Gen2 # 4	USB3.1 Gen1/Gen2 # 5	USB3.1 Gen1/Gen2 # 6	PCIE* # 7	PCIE* # 8	PCIE* # 9	PCIE* # 10	PCIE* # 11	PCIE* # 12	PCIE* # 13	PCIE* # 14	PCIE* # 15	PCIE* # 16
Intel® RST Support	No Support	No Support	No Support	No Support	No Support	No Support	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

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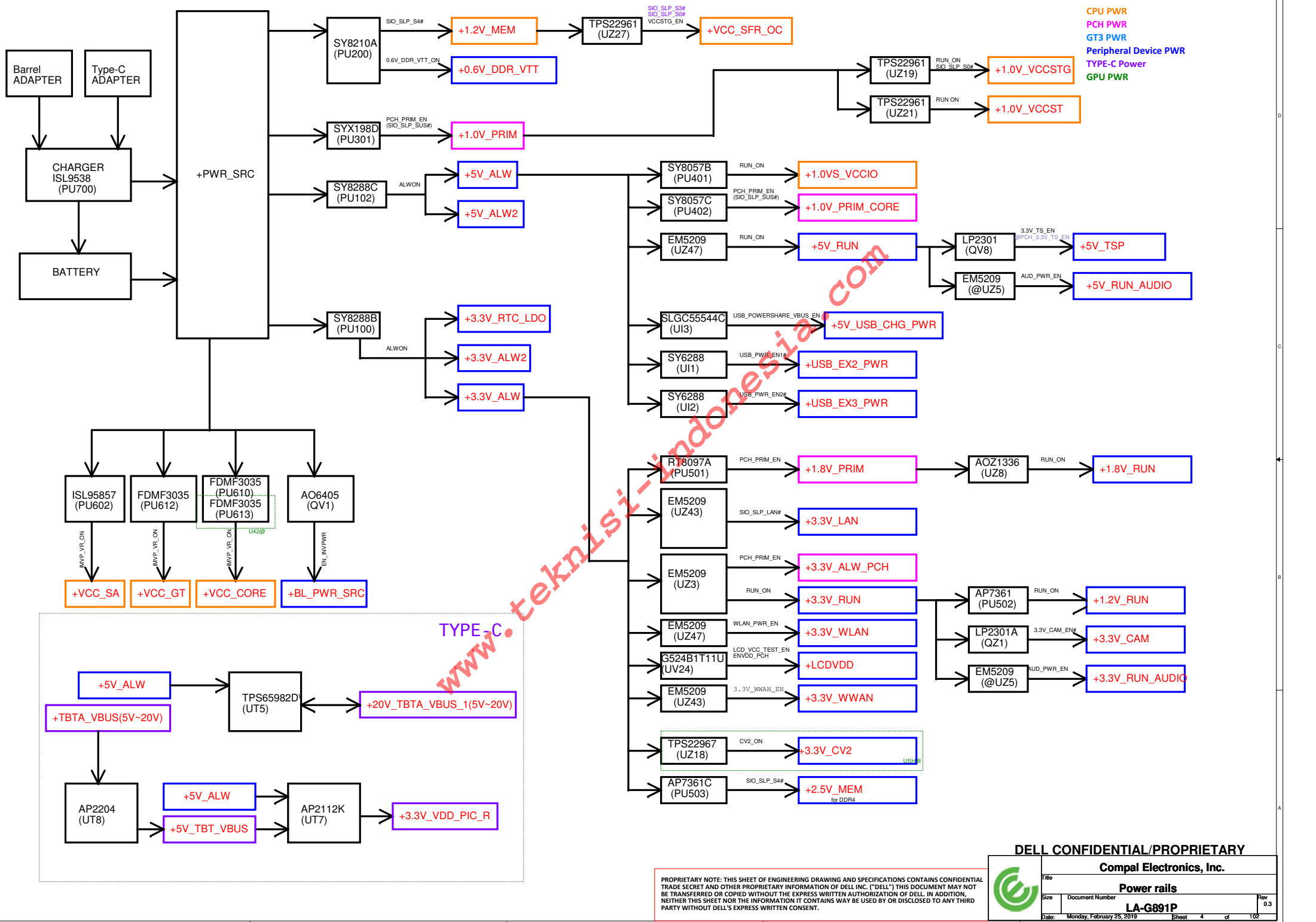
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Port assignment

LA-G891P

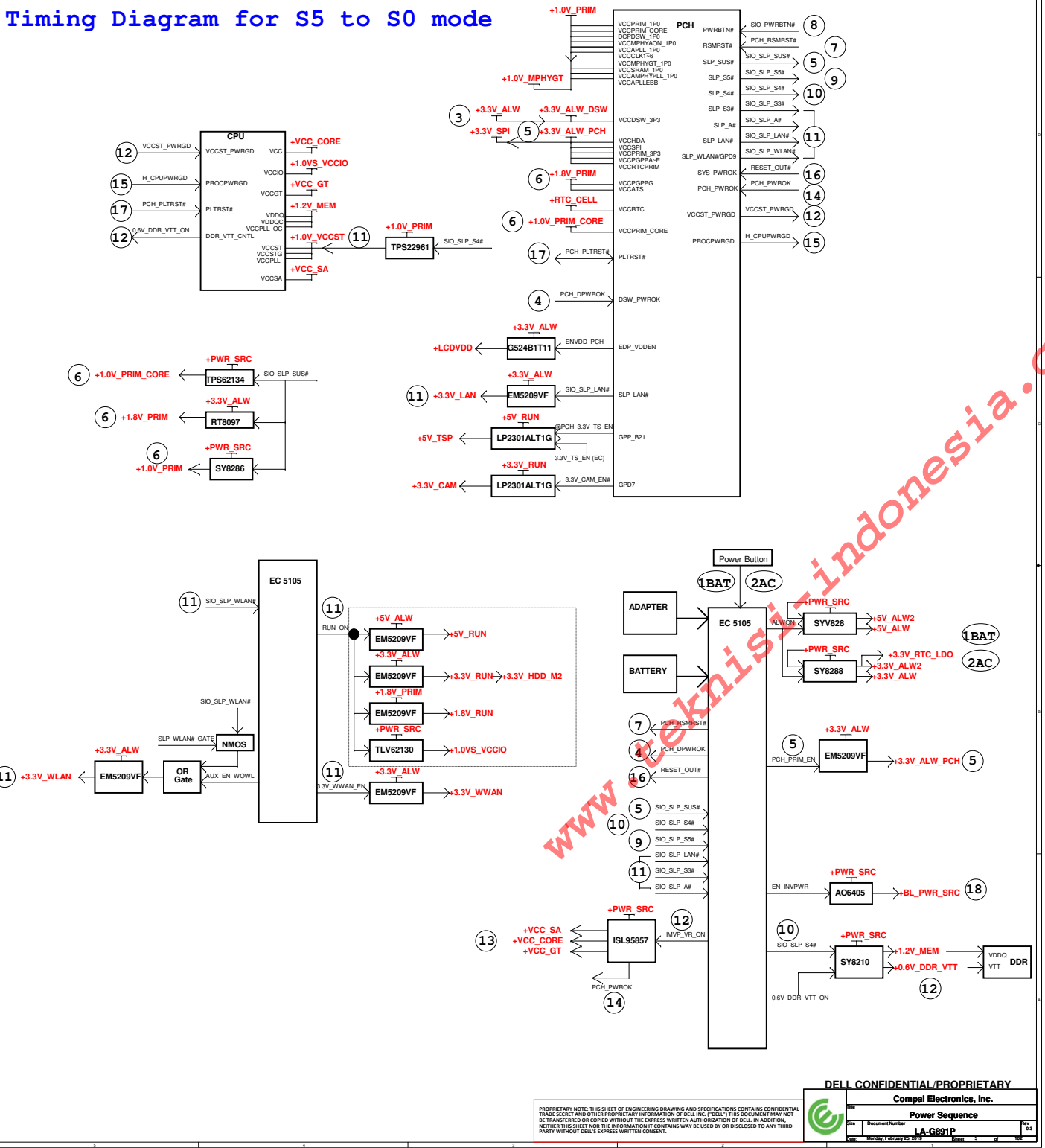


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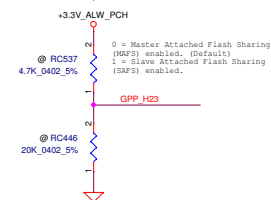
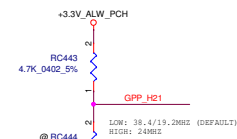
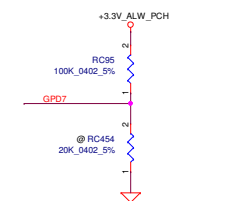
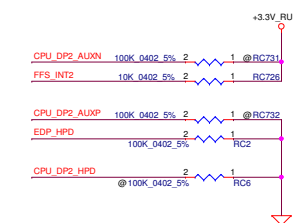
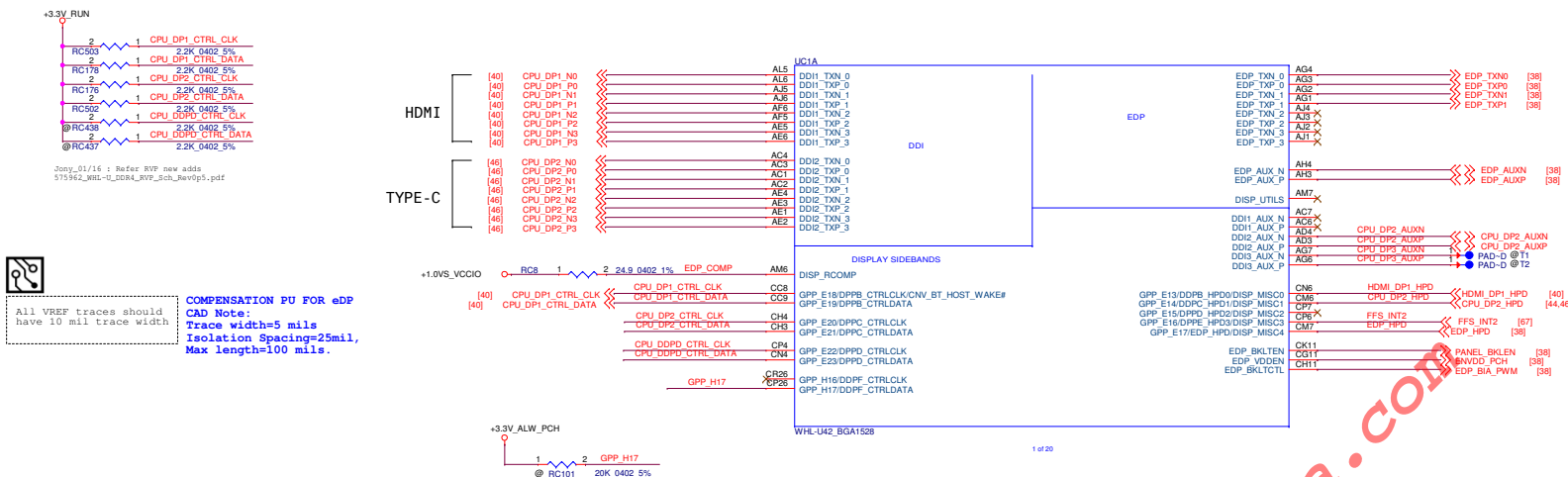
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Timing Diagram for S5 to S0 mode



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For 2LANE EDP



Vendor	JAE	FOXCON	TBD	TBD
TYPEC_CON_SEL1	LOW	LOW	HIGH	HIGH
TYPEC_CON_SEL2	LOW	HIGH	LOW	HIGH

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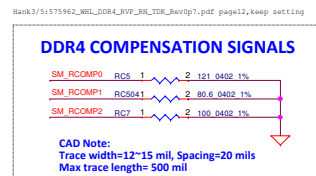
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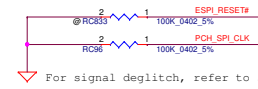
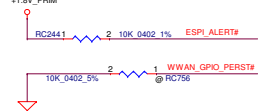
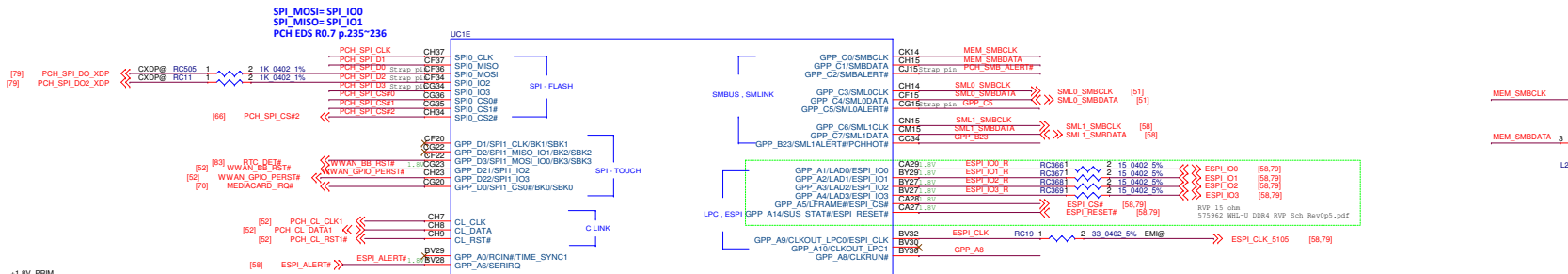
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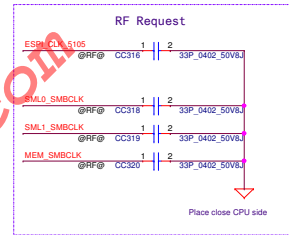
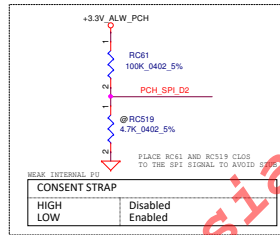
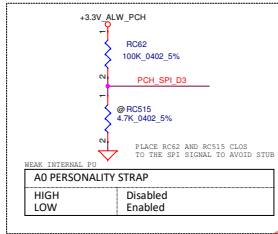
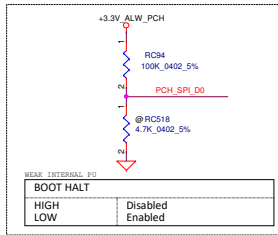
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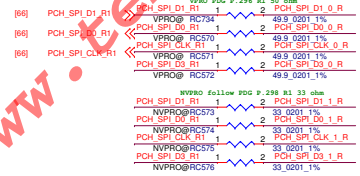




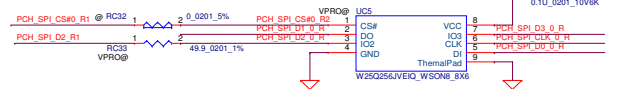
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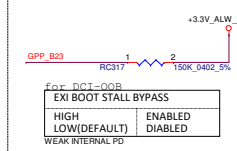
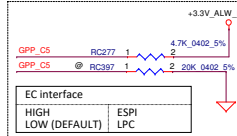
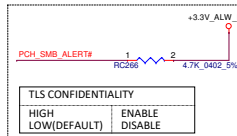
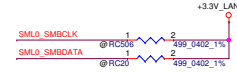
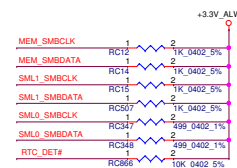
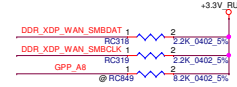
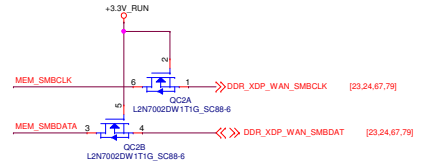
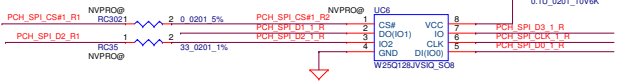
SOFTWARE TAA



For vPro 32MB WSON8 Flash ROM For Non-vPro 8MB WSON8 Flash ROM



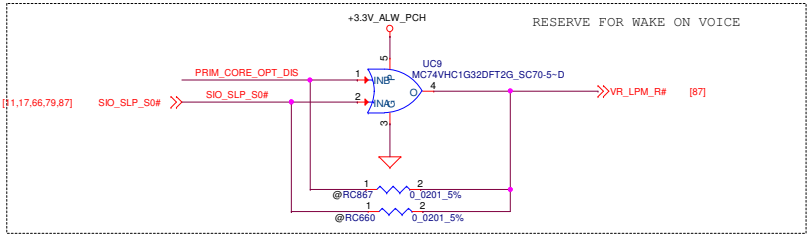
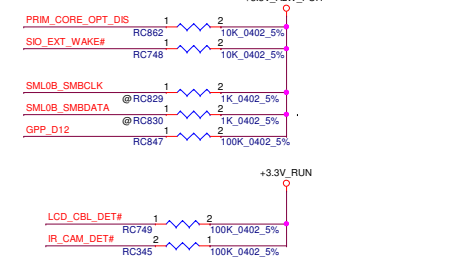
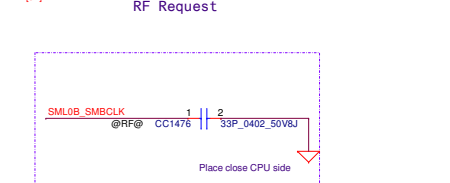
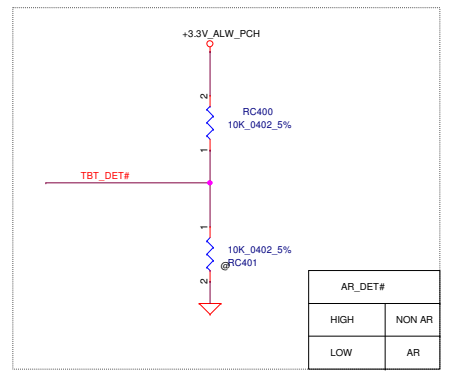
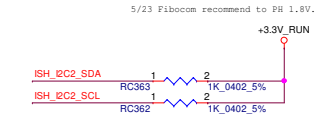
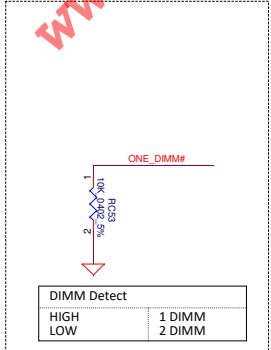
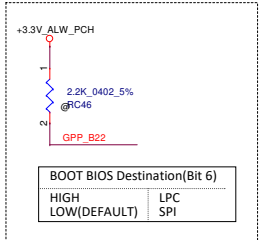
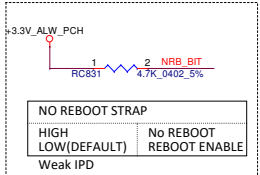
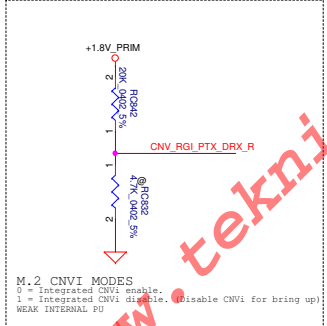
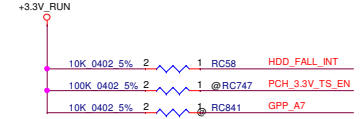
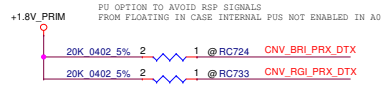
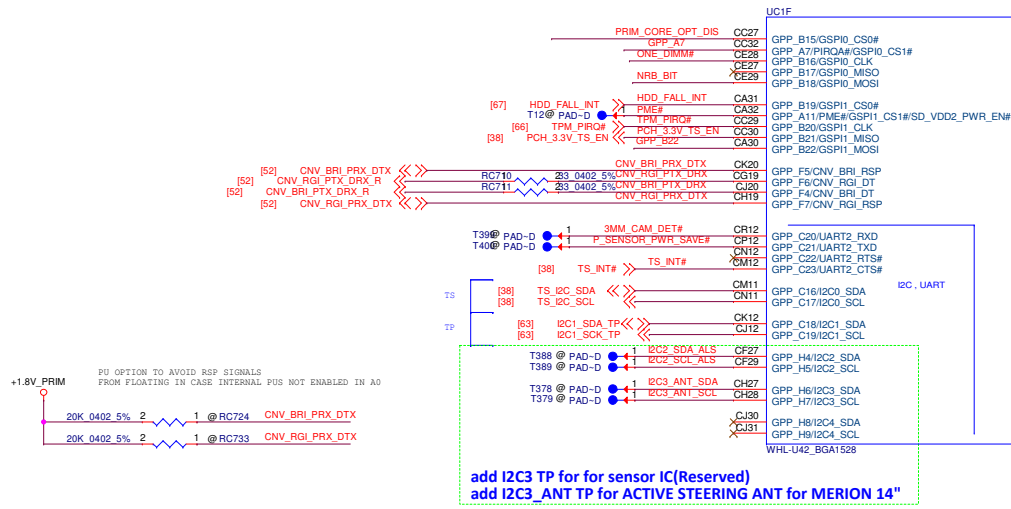
For Non-vPro 16MB SOP8 Flash ROM



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P09-MCP3(14)/SPI,SMB,LPC			
LA-G891P			
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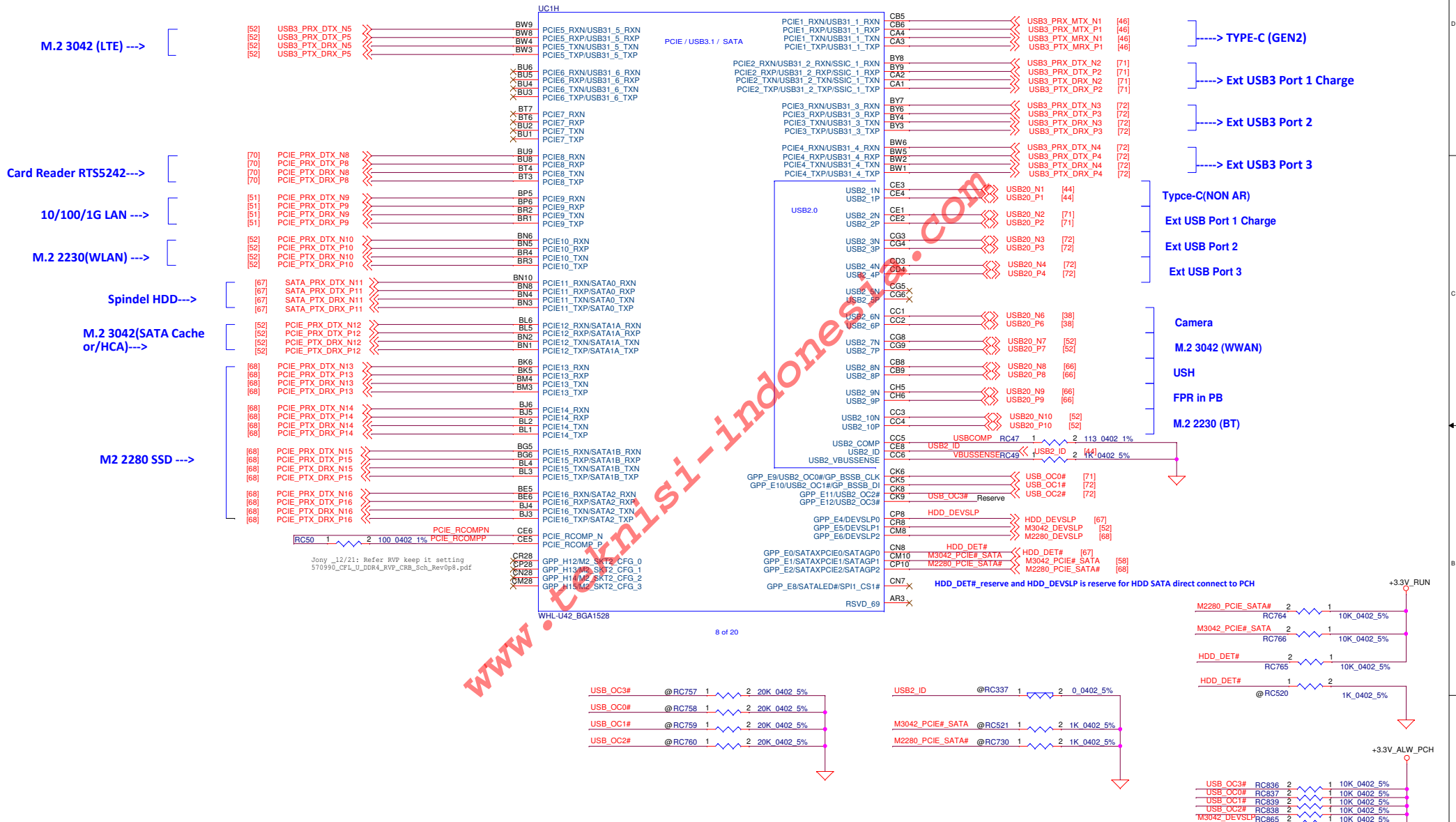


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Size	Document Number	Rev 0.3	
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AR,NB_Bandon DSC(follow WHL 180306C port map)

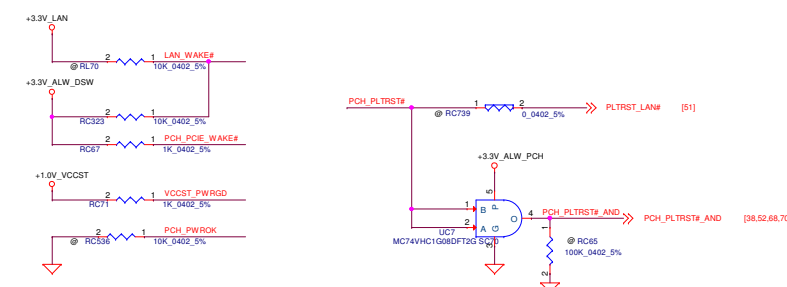
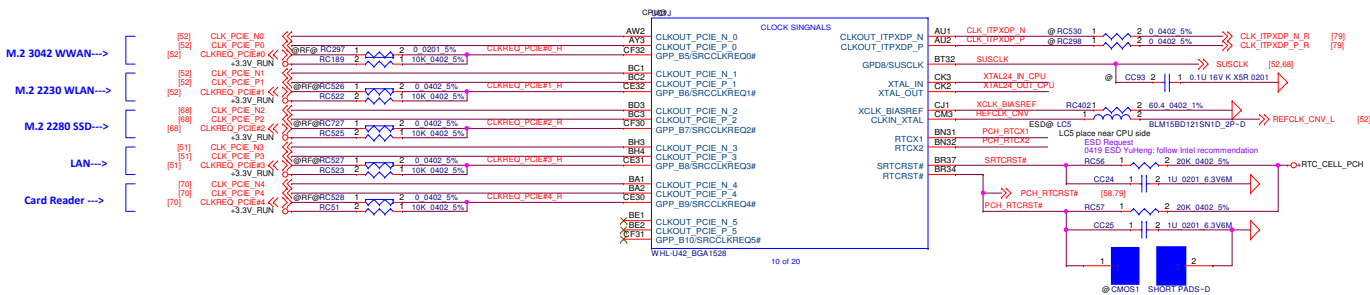
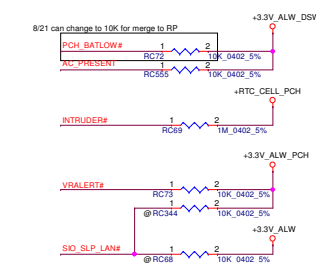


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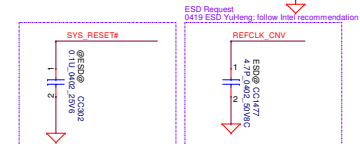
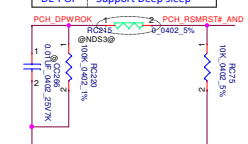


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Size	Document Number	Rev 0.3	
Date	Monday, February 25, 2019	Sheet	10 of 102

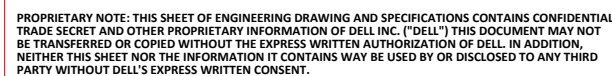
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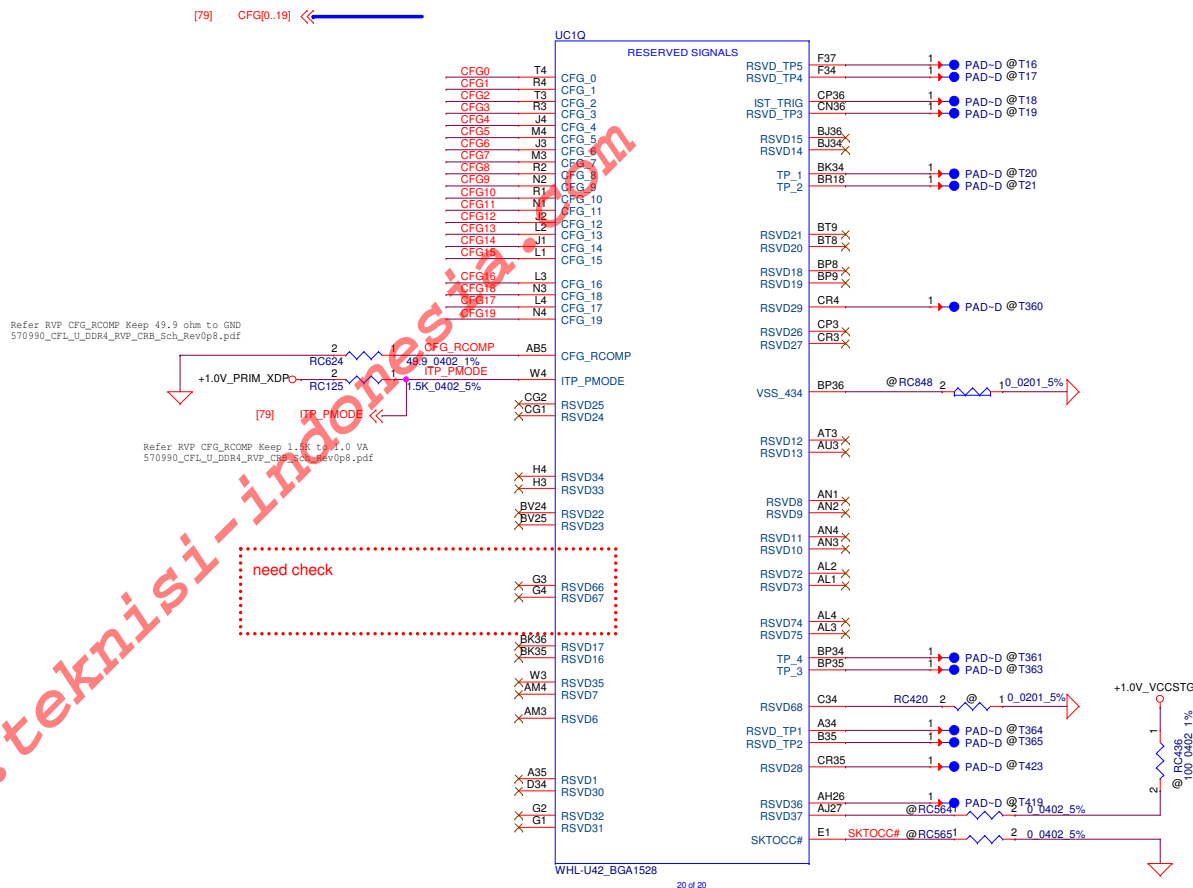
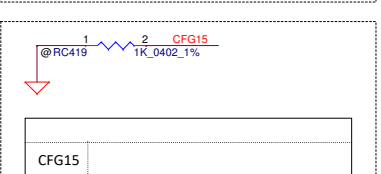
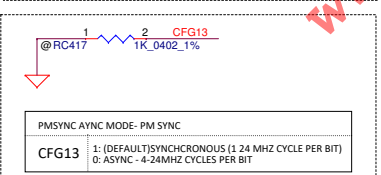
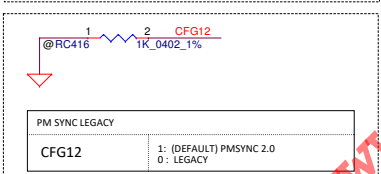
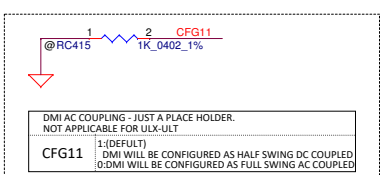
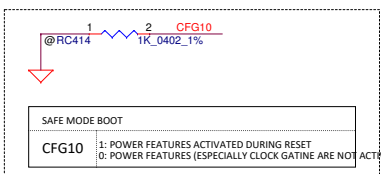
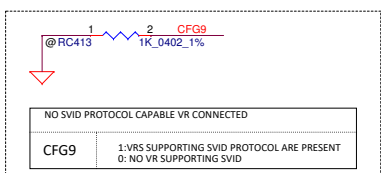
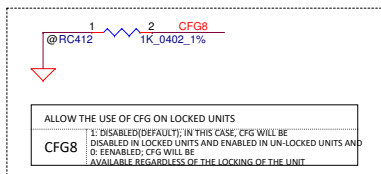
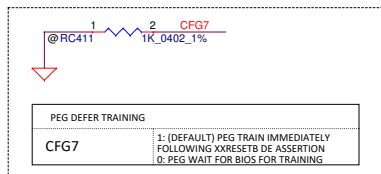
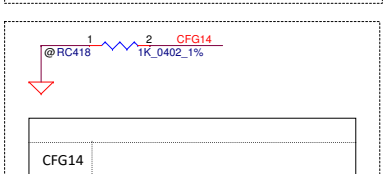
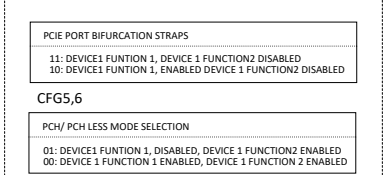
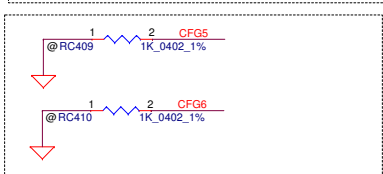
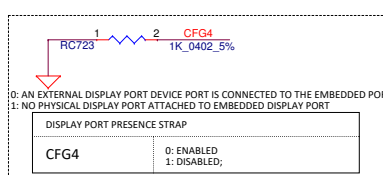
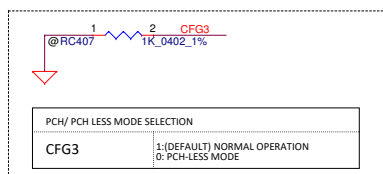
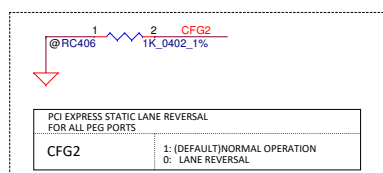
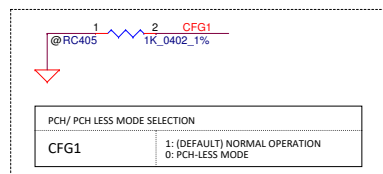
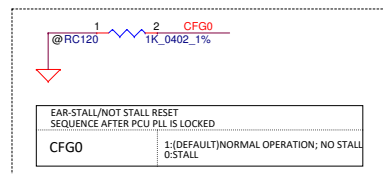
[illegible]

The diagram shows a signal line for **PCH_PLTRST# AND**. It includes an ESD protection component labeled **ESD @ CCI95** with parameters **.047U .0402 .16V7K**. The signal line is numbered **1** and **2** at the protection point. A note states: **For ESD solution**.



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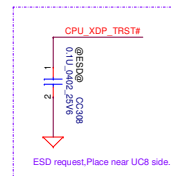
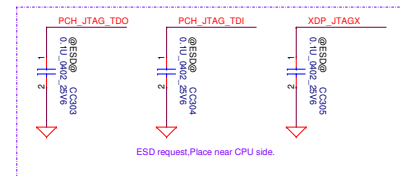
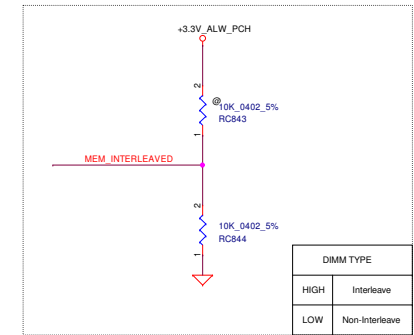
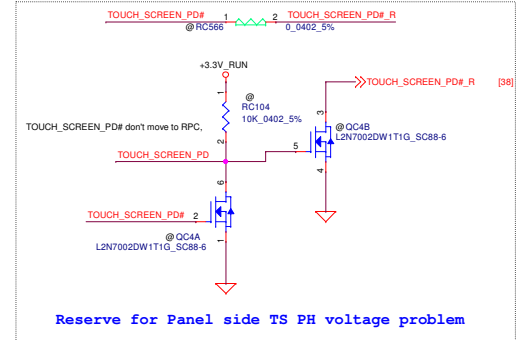
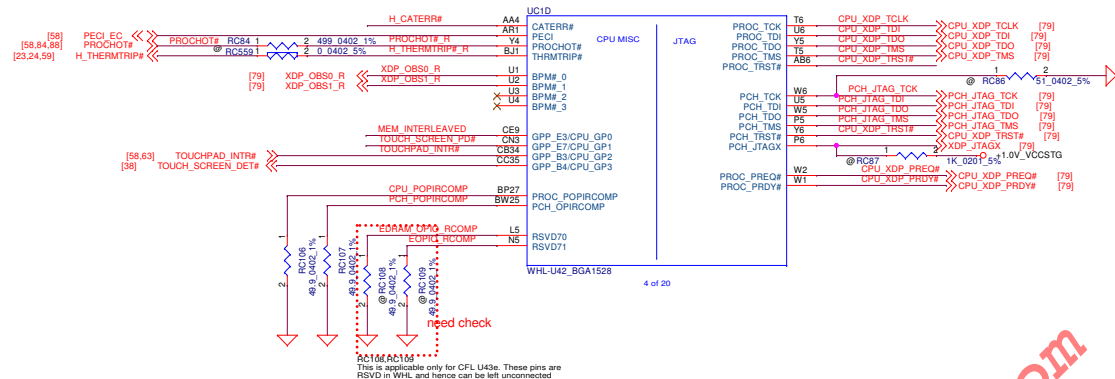
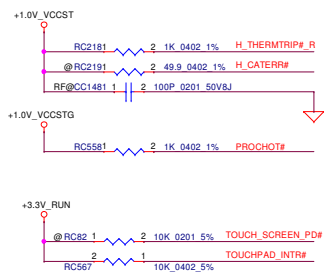
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P14-MCP(8/14)CFG.RSVD

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+V1.8S_EDRAM: 1.8V, 50mA - REMOVE
+VCC_EOPIO: 0.8~1V, 2A - REMOVE

T371@ PAD~D 1 +VCC_CORE_G0
T372@ PAD~D 1 +VCC_CORE_G1
T373@ PAD~D 1 +VCC_CORE_G2
T374@ PAD~D 1 +VCC_CORE_G3

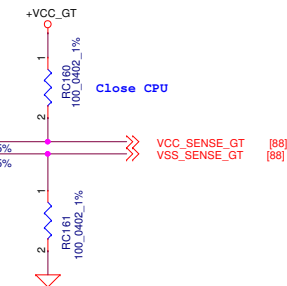
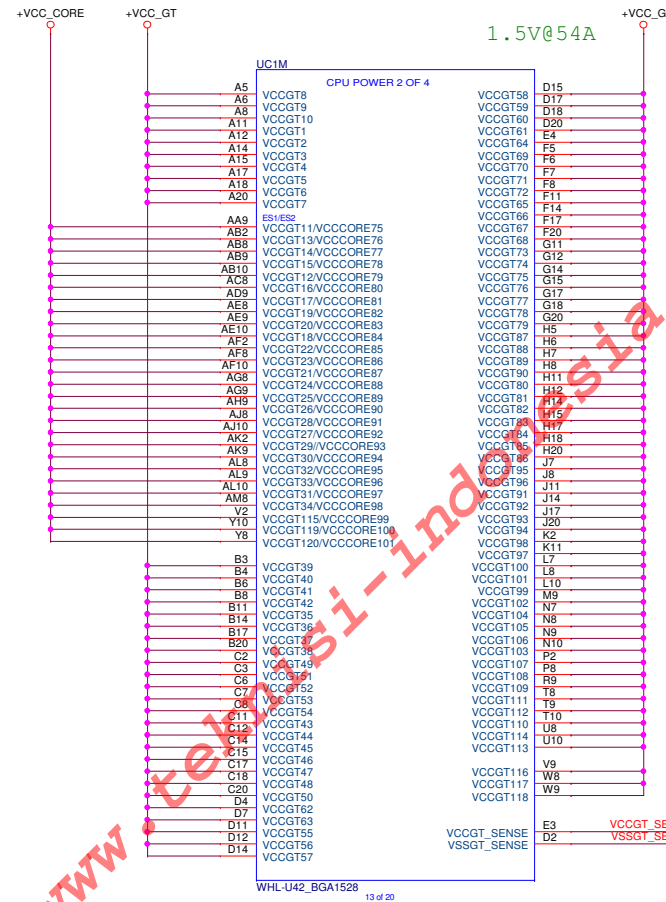


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THE BALLOUT ONLY FOR WHL ES2 CPU

+VCCGT: 0.55~1.5V, 54A
+VCCGTX : 0.55~1.5V, 7A

Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE

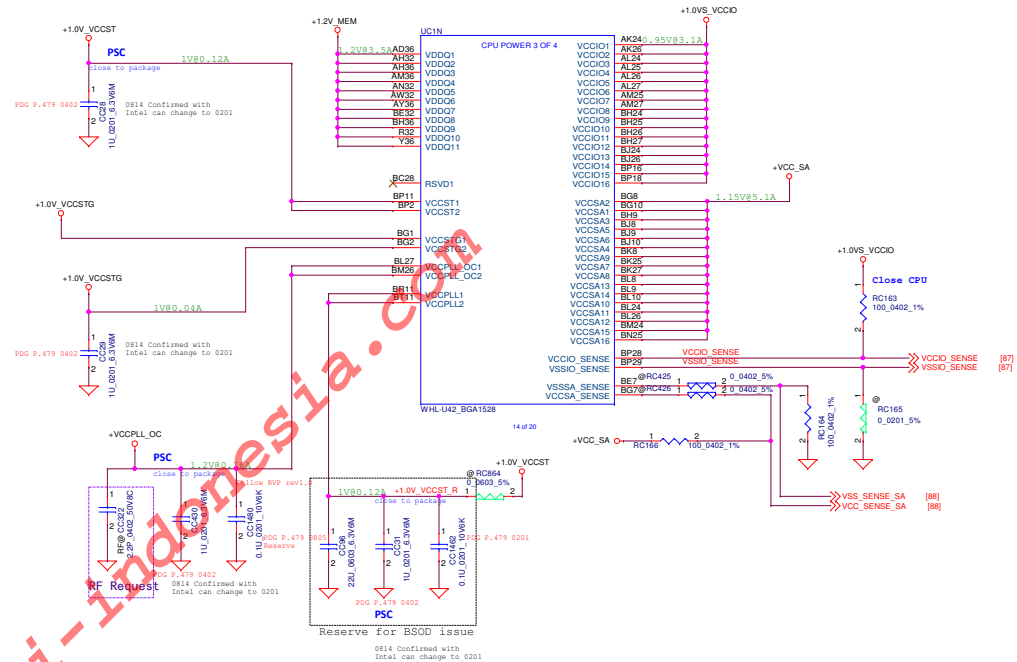


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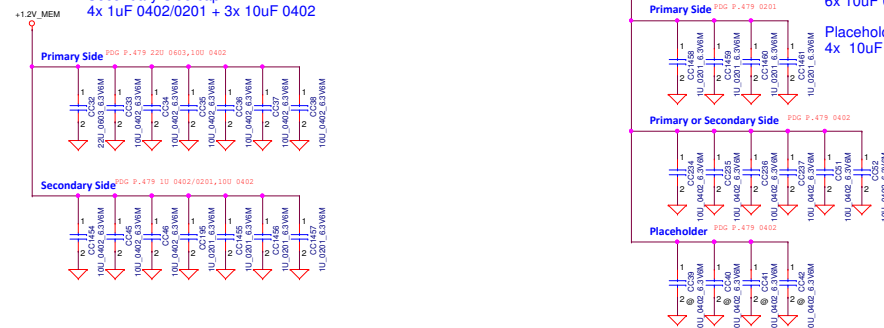


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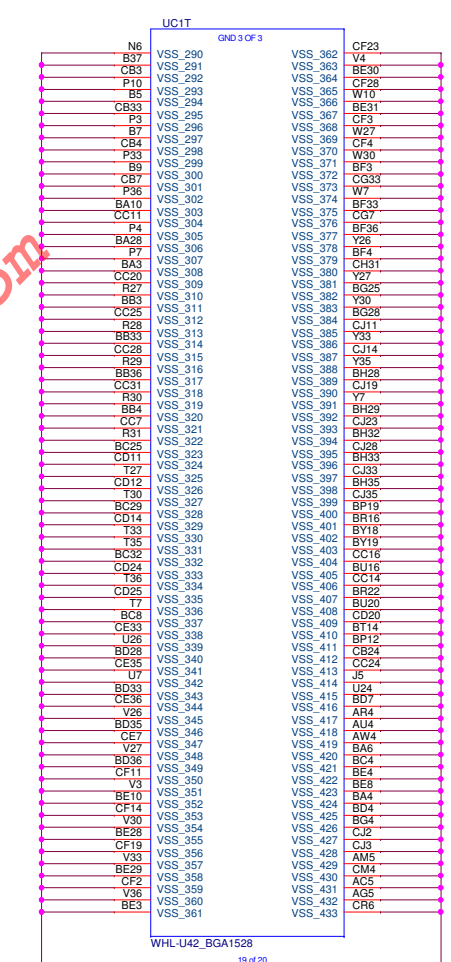
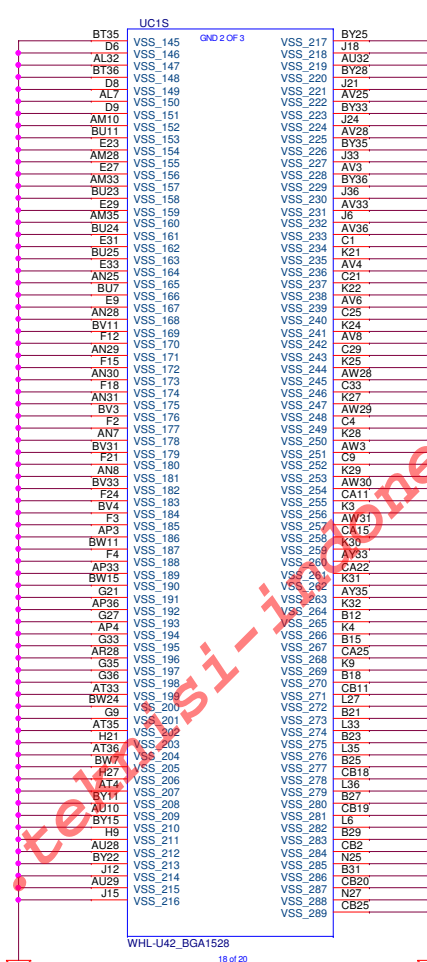
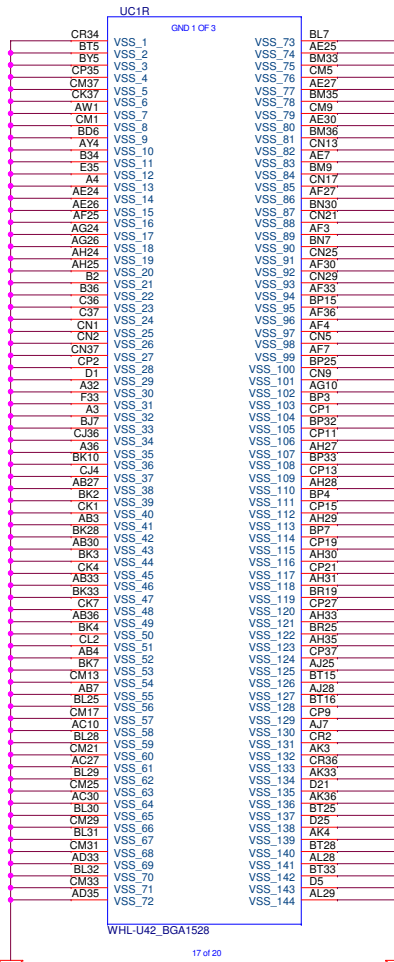


Placeholder Only
4x 10uF 0402




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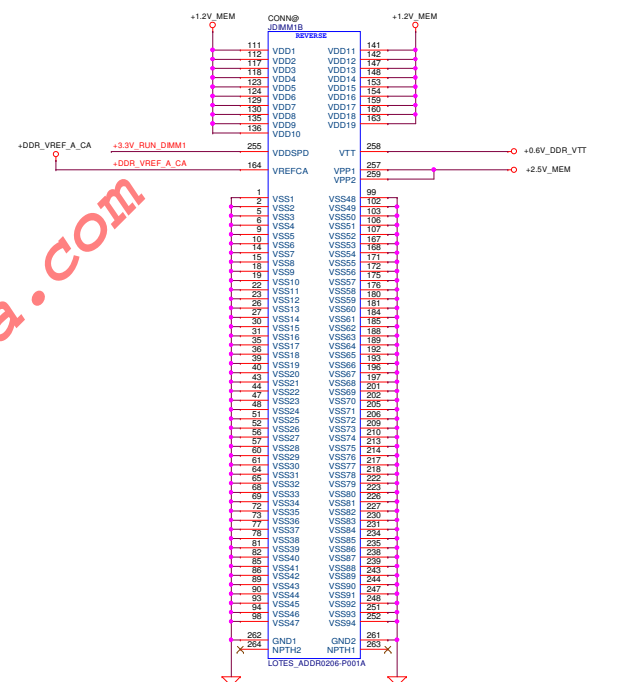
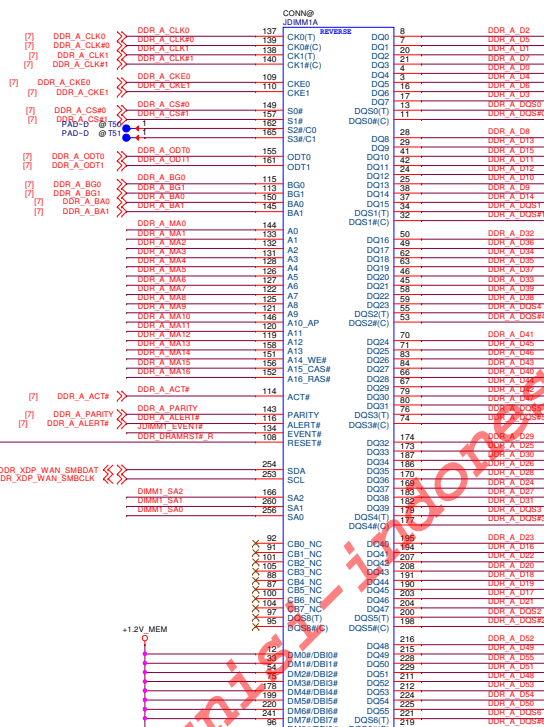
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Link LOTES_ADDR0206-P001A02 done 0410



WHL_U PDG rev0.8 P.92

VTT:

Place on VTT plane close to SODIMM

2x 10uF 0603(1 cap stuffed, 1 placeholder)

4x 1uF 0402

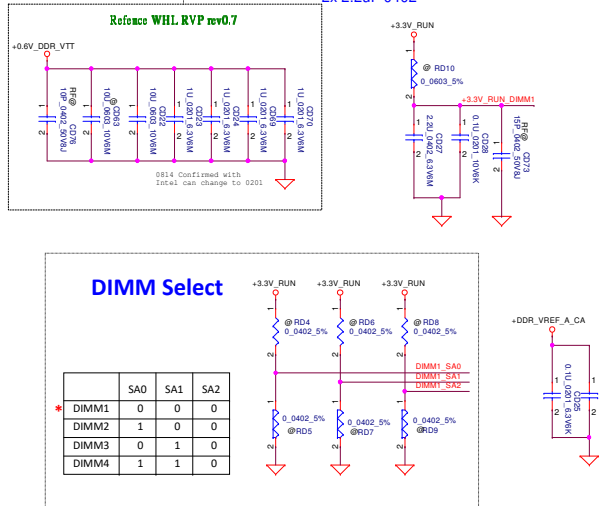
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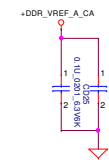
2x 0.1uF 0402

2x 2.2uF 0402

0.1uF



	SA0	SA1	SA2
* DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0



6/8 Change to SA00007WE00 DII

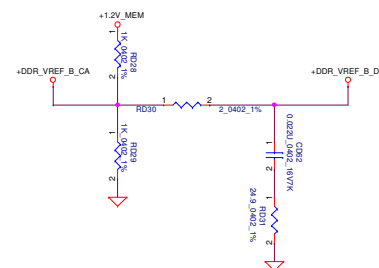
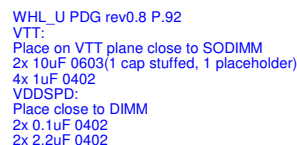
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Reference WHL RVP rev0.7



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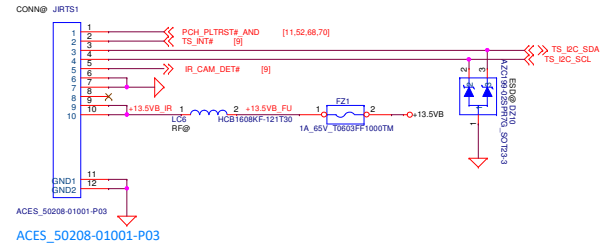


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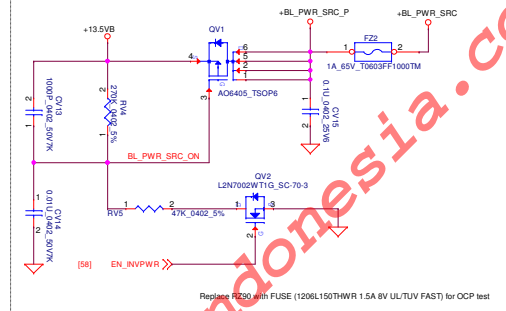
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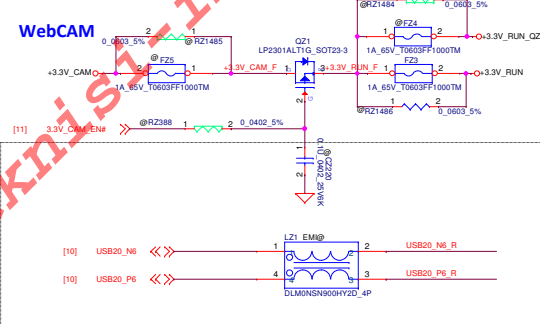
TOUCH SCREEN & IR CAMERA connector



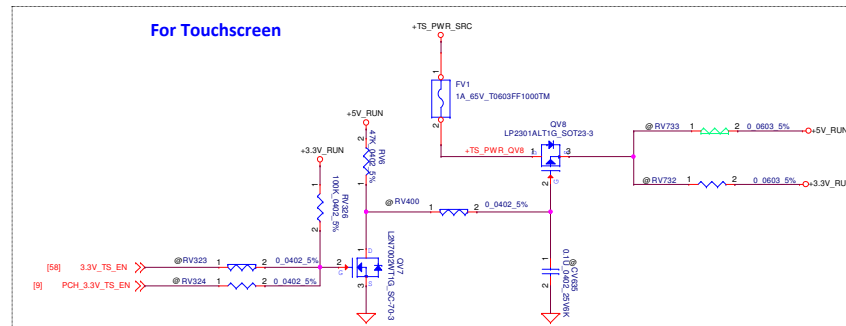
Backlight POWER



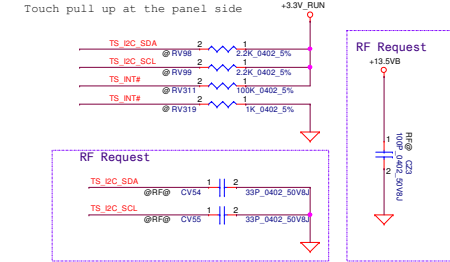
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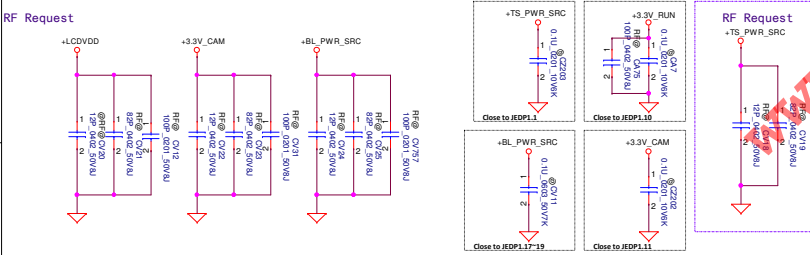
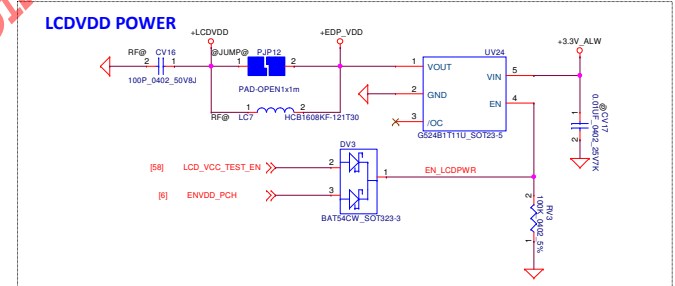
For Touchscreen



For 2LANE EDP &5V_TSP,NB15



LCDVDD POWER



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eDP CONN & Touch screen

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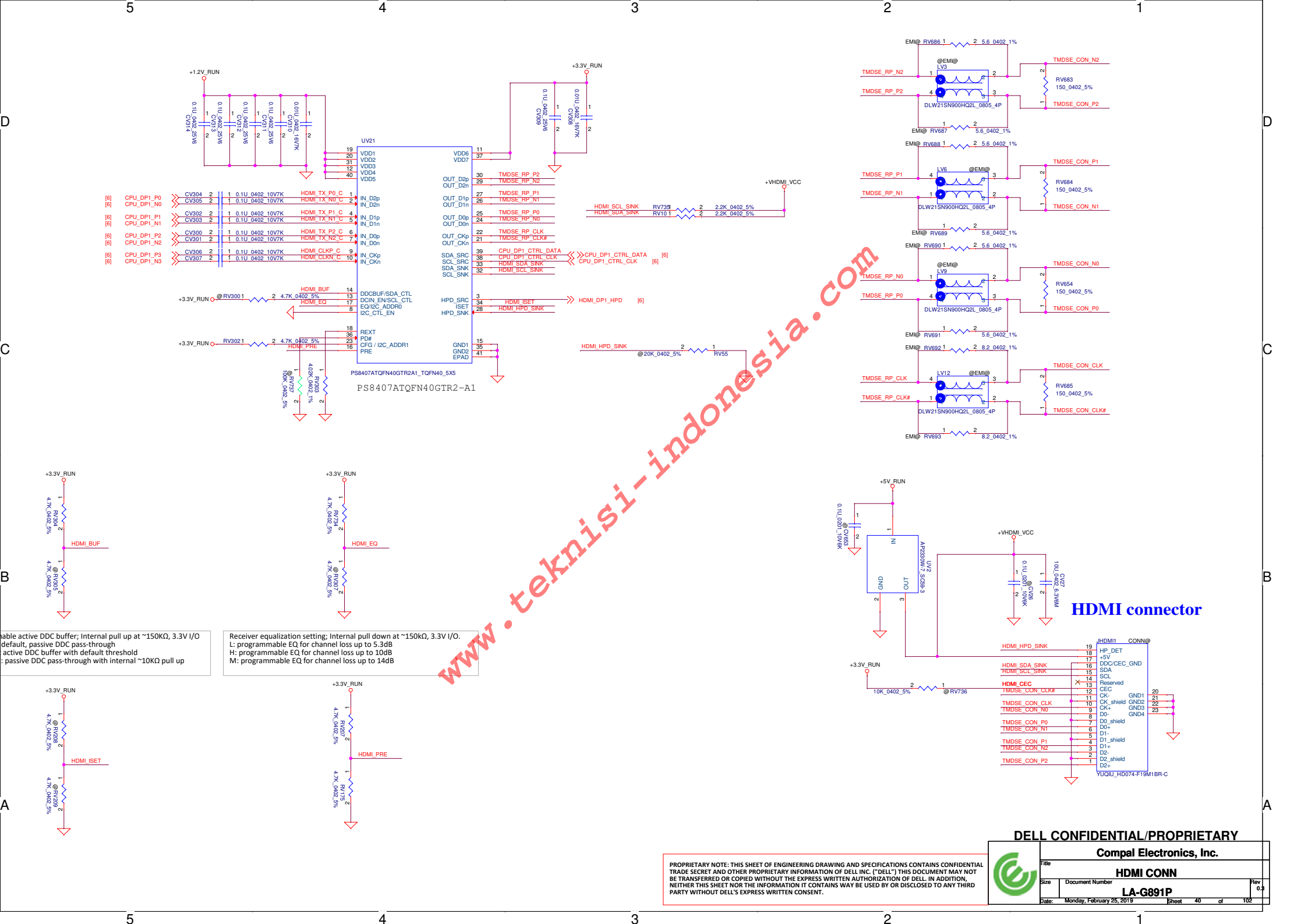
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Title			
TBT-AR-DP,PCIE			
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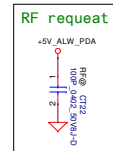
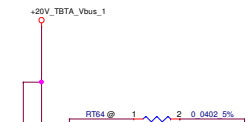
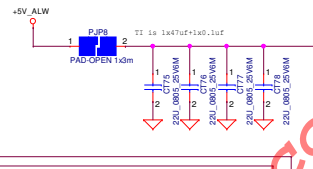
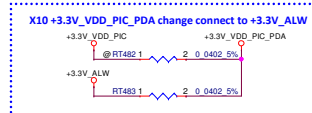
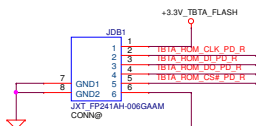
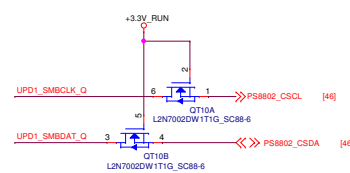
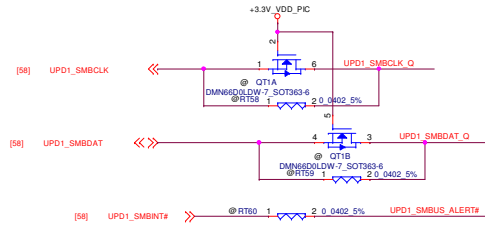
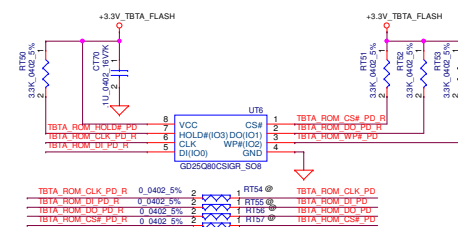


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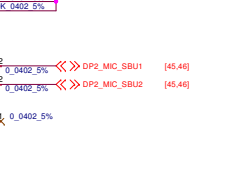
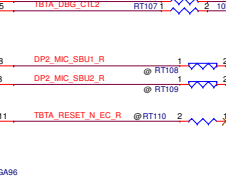
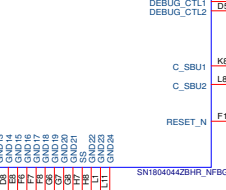
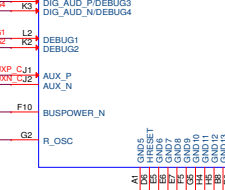
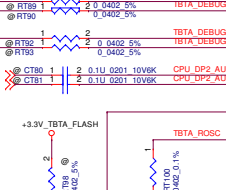
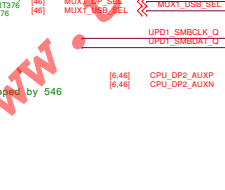
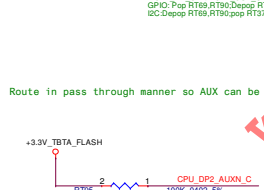
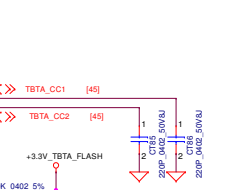
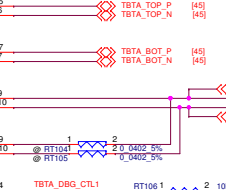
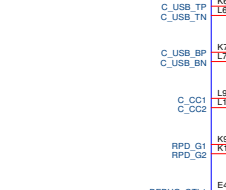
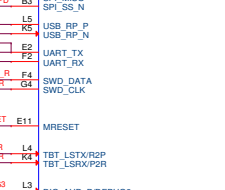
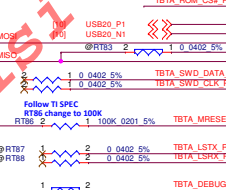
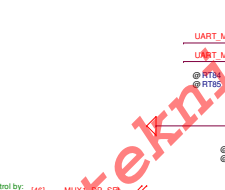
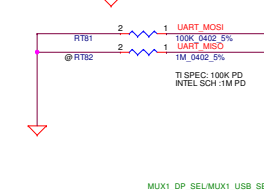
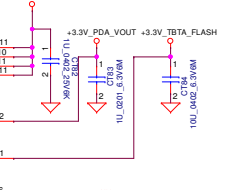
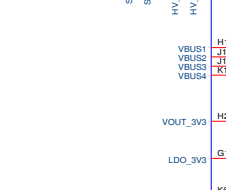
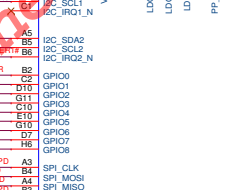
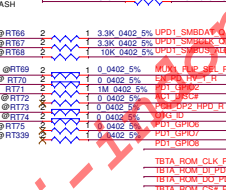
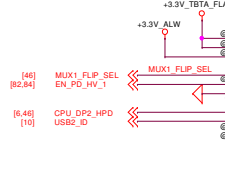
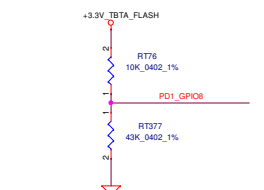
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Title		TBT-AR-VCC/VSS	
Size	Document Number		Rev
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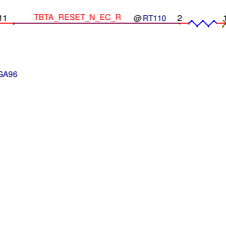
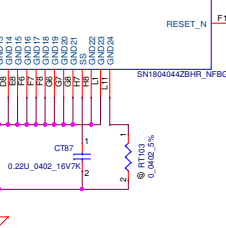
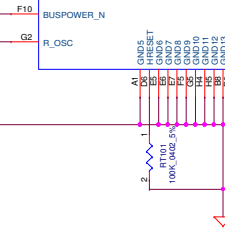
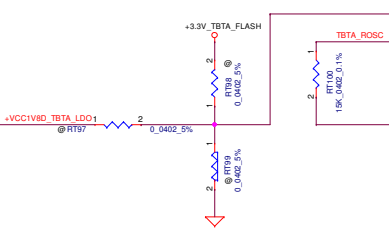
For Non-AR config



DIV = R2/(R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	<p>UFF only</p> <p>5V @0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes not supported</p> <p>T1 VID supported</p>
0.10	0.18	1	<p>UFF only</p> <p>5V @0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes -Sink, C and D pin configuration T1 VID supported</p>
0.20	0.28	2	<p>UFF only</p> <p>5V @0.9A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes not supported</p> <p>T1 VID supported</p>
0.30	0.38	3	<p>UFF only</p> <p>5V @0.9A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes -Sink, C and D pin configuration T1 VID supported</p>
0.40	0.48	4	<p>DPP</p> <p>5V @0.9-3.0A Sink capability</p> <p>5V @0.9A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes not supported</p> <p>T1 VID supported</p> <p>Accepts data and power role swaps, but does not initiate.</p>
0.50	0.58	5	<p>DPP</p> <p>5V @0.9-3.0A Sink capability</p> <p>5V @0.9A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes - Source, C, D, and E pin configurations.</p> <p>T1 VID supported</p> <p>Accepts power role swaps but will not initiate.</p> <p>Accepts data role swaps to UFP and can initiate.</p>
0.60	0.68	6	<p>DPP</p> <p>5V @0.9-3.0A Sink capability</p> <p>5V @0.9A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes - Source, C, D, and E pin configurations.</p> <p>T1 VID supported</p> <p>Accepts power role swaps but will not initiate.</p> <p>Accepts data role swaps to DPP and can initiate.</p>
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.



Route in pass through manner so AUX can be snooped by 546



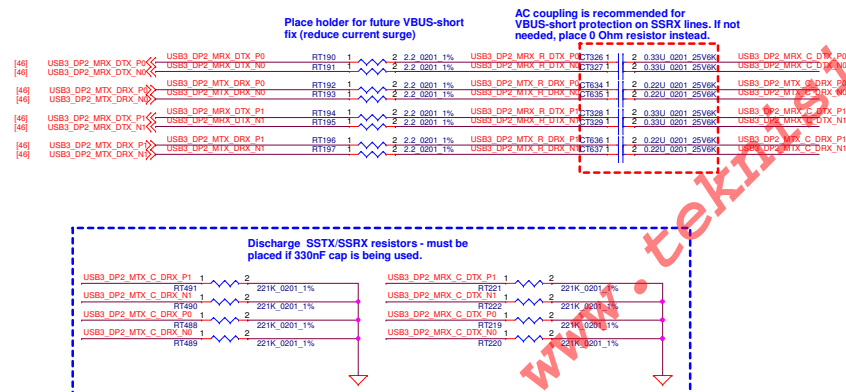
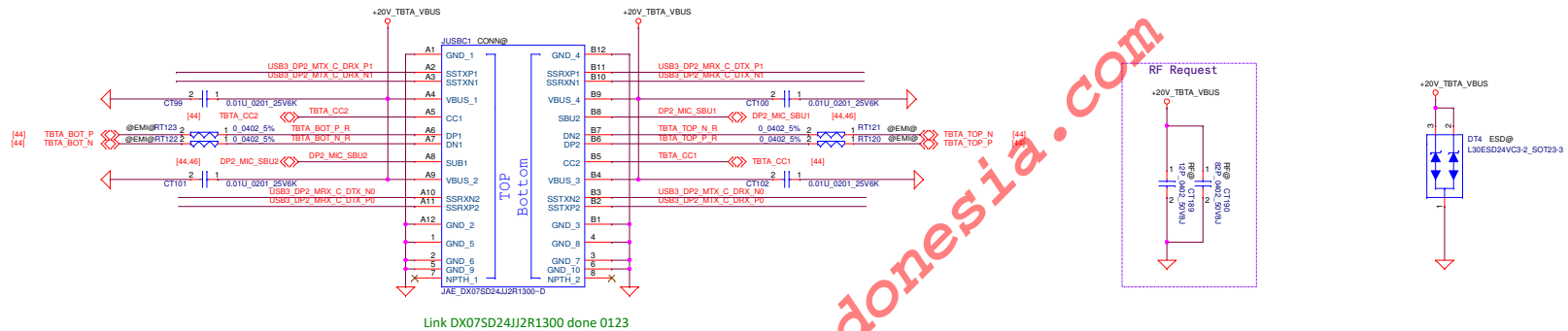
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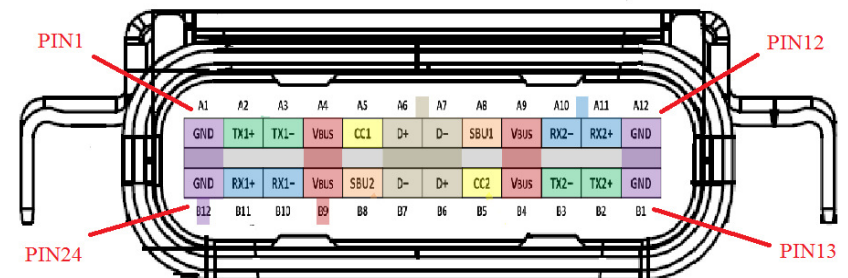
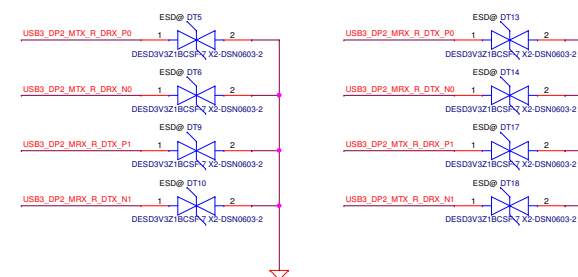
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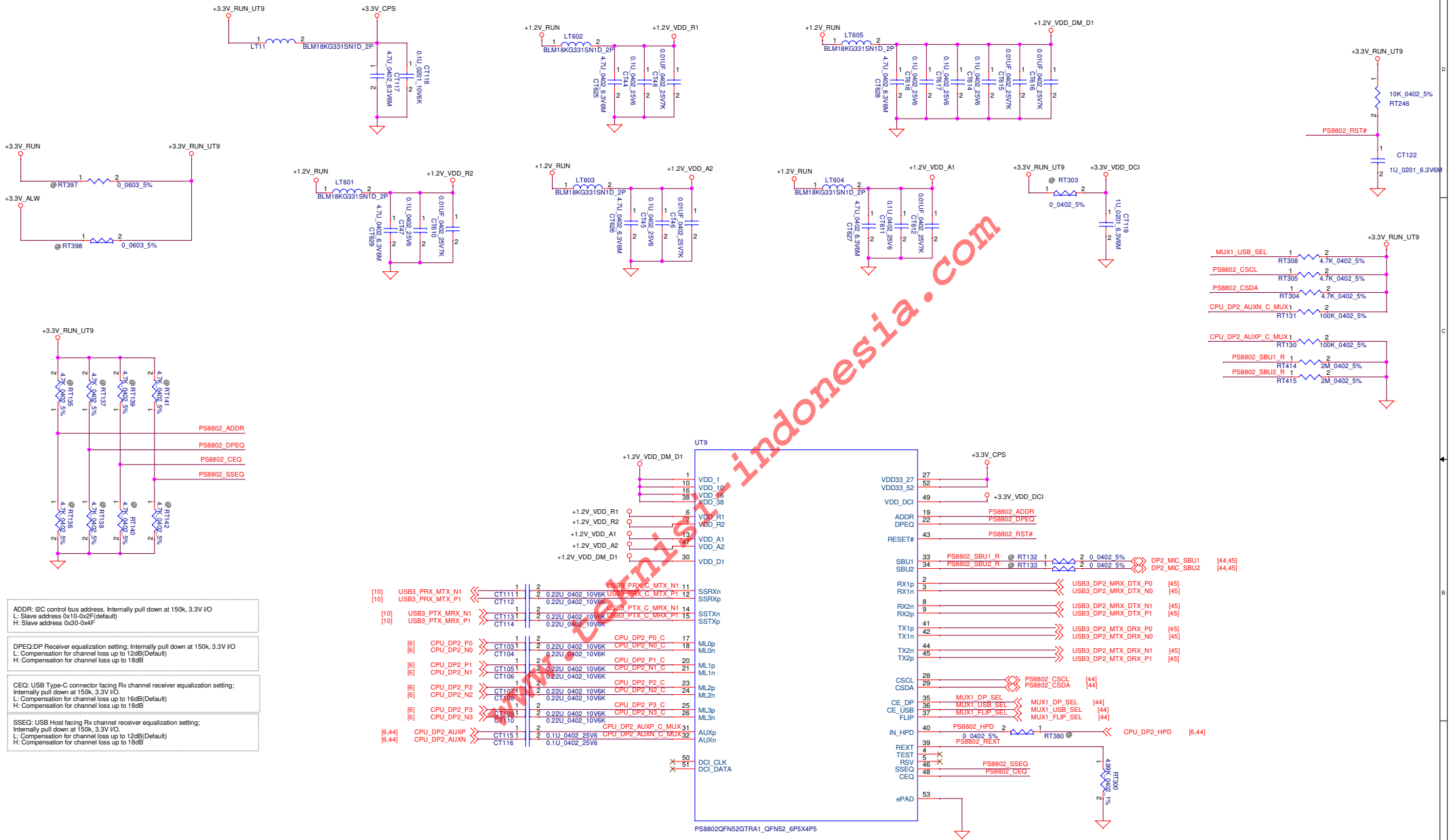
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CT630-633 use SD043000080 (0 ohm) for CSLP3 build



change typeC ESD part from SC40000AR00 to SC40000DF00





ADDR: I2C control bus address. Internally pull down at 150k, 3.3V I/O
 L: Slave address 0x10-0x0F (Default)
 H: Slave address 0x30-0x4F

DPEQ: DP Receiver equalization setting. Internally pull down at 150k, 3.3V I/O
 L: Compensation for channel loss up to 12dB (Default)
 H: Compensation for channel loss up to 18dB

CEQ: USB Type-C connector facing Rx channel receiver equalization setting;
 Internally pull down at 150k, 3.3V I/O
 L: Compensation for channel loss up to 16dB (Default)
 H: Compensation for channel loss up to 18dB

SSEQ: USB Host facing Rx channel receiver equalization setting;
 Internally pull down at 150k, 3.3V I/O
 L: Compensation for channel loss up to 12dB (Default)
 H: Compensation for channel loss up to 18dB

[10]	USB3_PRX_MTX_N1	CT1111	2	0.22u 0402 10V6K	USB3_PTX_C_MTX_N1	11	1
[10]	USB3_PRX_MTX_P1	CT1112	2	0.22u 0402 10V6K	USB3_PTX_C_MTX_P1	12	1
[10]	USB3_PTX_MRX_N1	CT1113	2	0.22u 0402 10V6K	USB3_PTX_C_MRX_N1	14	1
[10]	USB3_PTX_MRX_P1	CT1114	2	0.22u 0402 10V6K	USB3_PTX_C_MRX_P1	15	1
[6]	CPU_DP2_P0	CT1031	2	0.22u 0402 10V6K	CPU_DP2_P0_C	17	1
[6]	CPU_DP2_N0	CT104	2	0.22u 0402 10V6K	CPU_DP2_N0_C	18	1
[6]	CPU_DP2_P1	CT1051	2	0.22u 0402 10V6K	CPU_DP2_P1_C	20	1
[6]	CPU_DP2_N1	CT106	2	0.22u 0402 10V6K	CPU_DP2_N1_C	21	1
[6]	CPU_DP2_P2	CT1071	2	0.22u 0402 10V6K	CPU_DP2_P2_C	23	1
[6]	CPU_DP2_N2	CT108	2	0.22u 0402 10V6K	CPU_DP2_N2_C	24	1
[6]	CPU_DP2_P3	CT1091	2	0.22u 0402 10V6K	CPU_DP2_P3_C	25	1
[6]	CPU_DP2_N3	CT110	2	0.22u 0402 10V6K	CPU_DP2_N3_C	26	1
[6,44]	CPU_DP2_AUXP	CT1151	2	0.1u 0402 25V6	CPU_DP2_AUXN_C_MUX1	31	1
[6,44]	CPU_DP2_AUXN	CT1116	2	0.1u 0402 25V6	CPU_DP2_AUXN_C_MUX2	32	1

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Title

TYPE-C

Size

Document Number

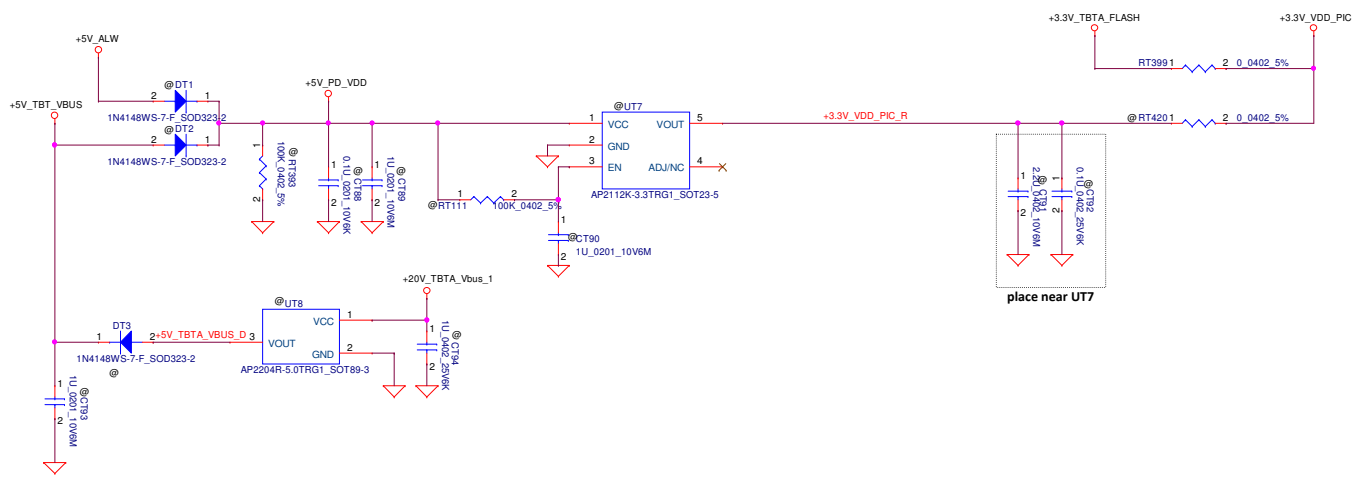
LA-G891P

Rev

0.3

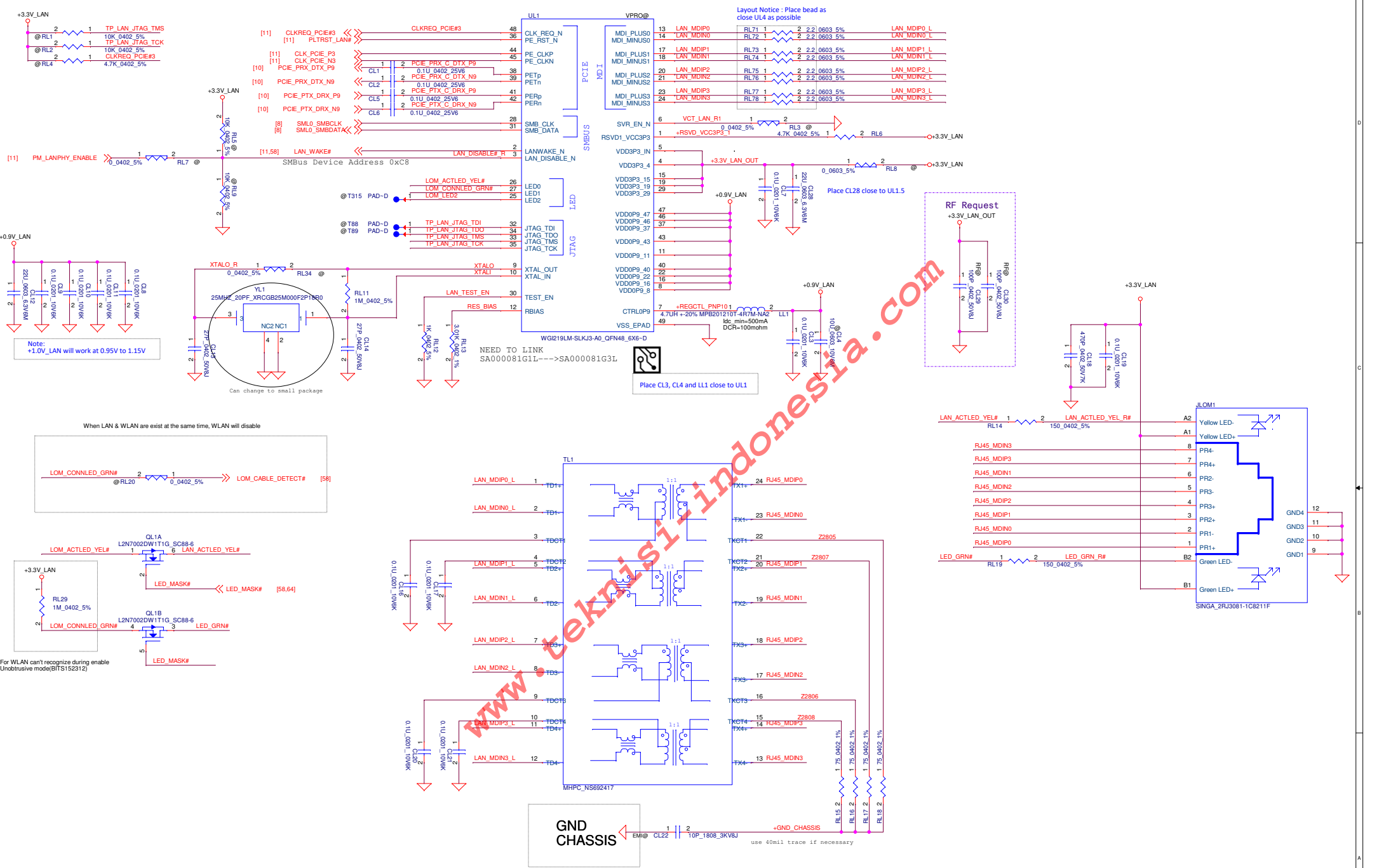
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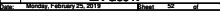
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2017/01/01		2018/01/01		[Type C]PD Power	
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NGFF slot E Key E



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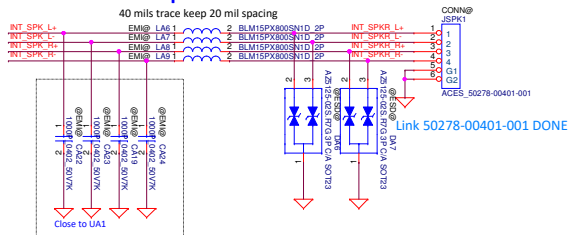


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Title			
PCIE device			
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1W x 1ch, 4ohm (Transducer spec is 80mm/0.5Watt per unit, there are two transducer units in one speaker box)

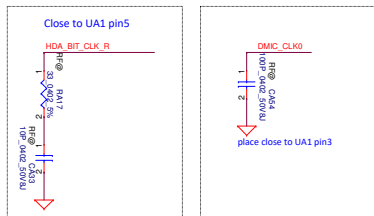
Internal Speakers Header

40 mils trace keep 20 mil spacing

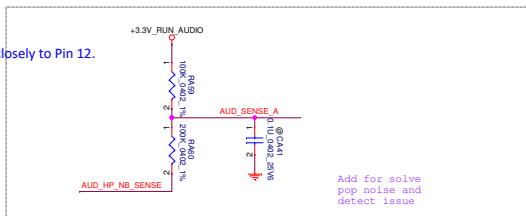


Link 50278-00401-001 DONE

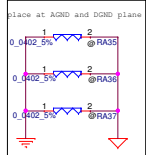
Close to UA1 pin5



Place closely to Pin 12.

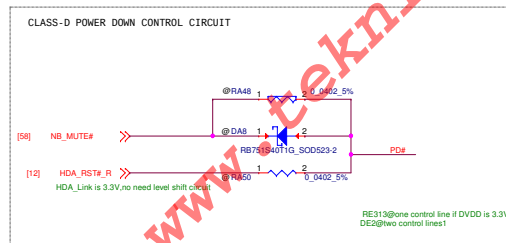


Add for solve pop noise and detect issue



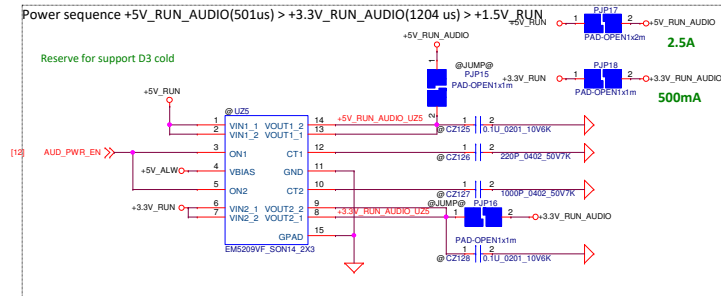
place at AGND and DGND plane

CLASS-D POWER DOWN CONTROL CIRCUIT

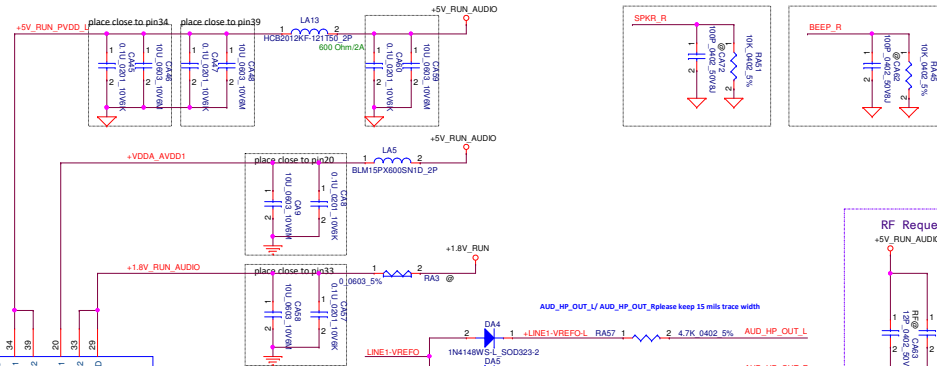


RE313@one control line if DVDD is 3.3V
DE2@two control lines!

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN_AUDIO



Reserve for support D3 cold



place close to pin34, place close to pin39, place close to pin8, place close to pin1, place close to pin20, place close to pin33, place near Codec

AUD_HP_OUT_L/AUD_HP_OUT_Release keep 15 mils trace width, AUD_HP_OUT_L/AUD_HP_OUT_Release keep 15 mils trace width, AUD_HP_OUT_L/AUD_HP_OUT_Release keep 15 mils trace width

HP-Out-Right, HP-Out-Left, Nokia-MIC, iPhone-MIC, Global Headset, Universal Jack

RF Request +5V_RUN_AUDIO, RF Request +1.8V_RUN, RF Request +3.3V_RUN_AUDIO

Place CA29 close to Codec, 0805 change to 10 0201*2 for MLCC shortage only Samsung,Taiyo,Murata can use

Place CA29/CA76 close to Codec

Place this Filter to avoid other components/chips be influenced

EMI changes value, need to inform vendor first

Reserve for support D3 cold

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN_AUDIO

Reserve for support D3 cold

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Compal Electronics, Inc.

Codec ALC3204

LA-G891P

Date: Monday, February 25, 2019 Sheet 56 of 102

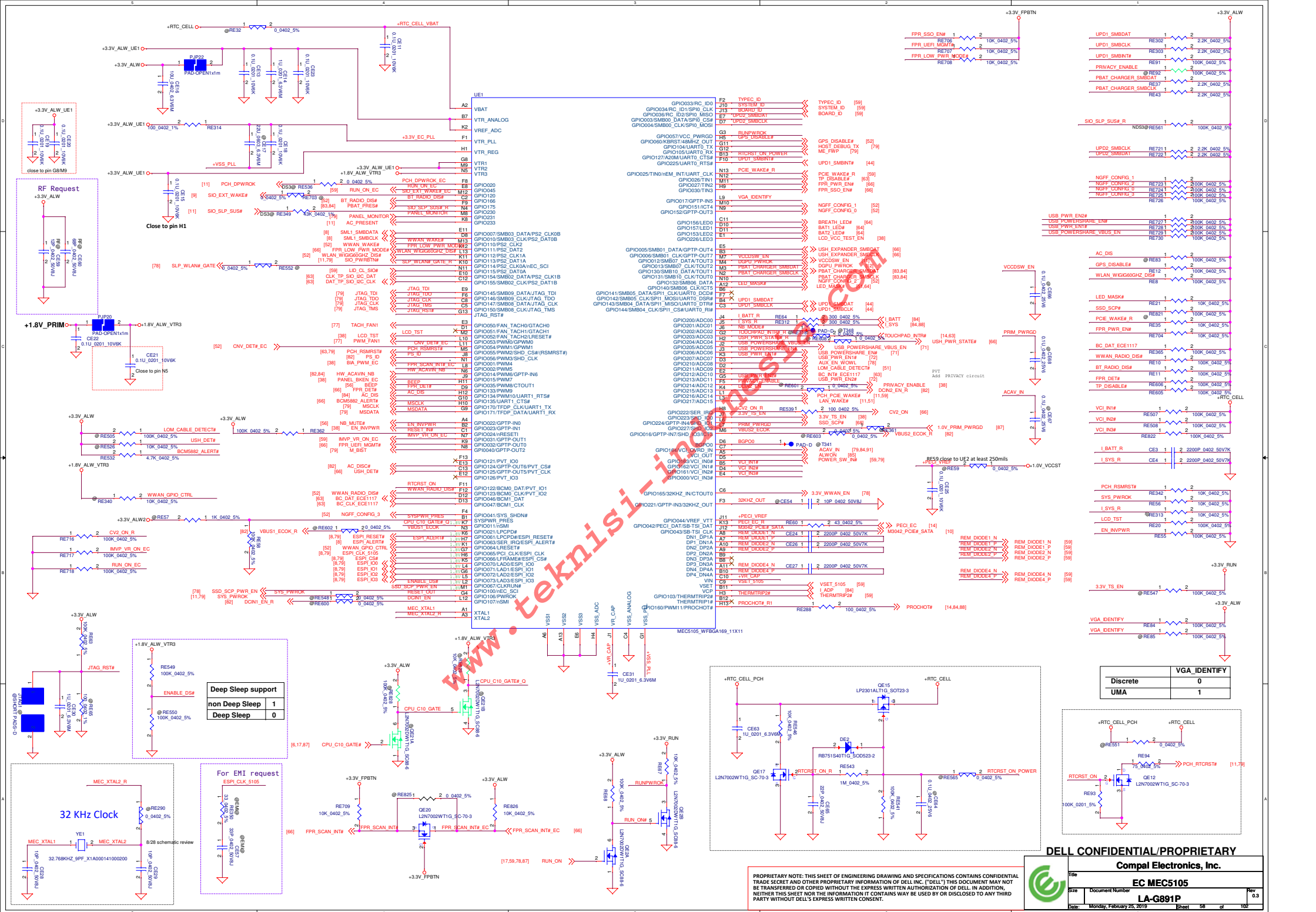
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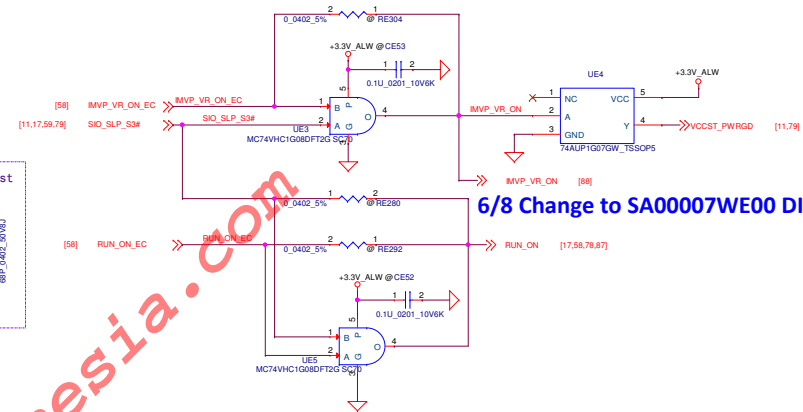
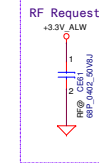
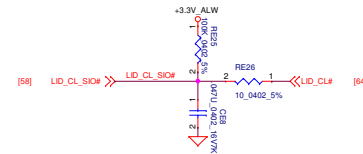
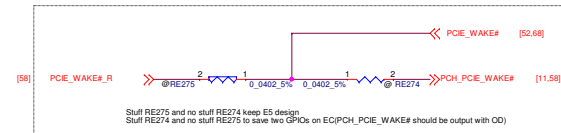
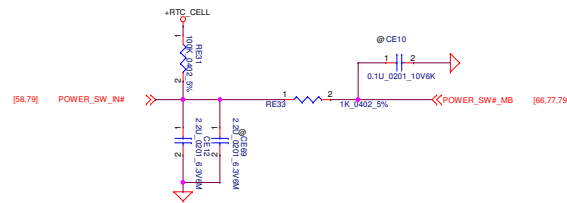
Reserve

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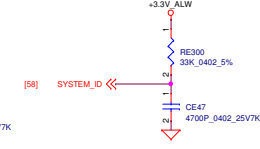
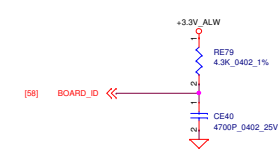
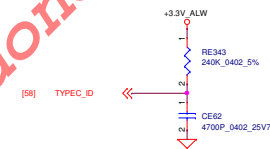


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Compal Electronics, Inc.		
Title		
Audio Amplifier		
Size	Document Number	Rev
	LA-G891P	0.3
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6/8 Change to SA00007WE00 DII



RE343	CE62	REV
* 240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	.
2K	4700p	.
1K	4700p	.

RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	reserved
* 4.3K	4700p	A00
2K	4700p	.
1K	4700p	.

RE300	CE47	PANEL SIZE
240K	4700p	11"
130K	4700p	12"
62K	4700p	13"
* 33K	4700p	14"
8.2K	4700p	15"
4.3K	4700p	17"
2K	4700p	15P
1K	4700p	.

PD ACE_DET# rise time is measured from 5%~68%.

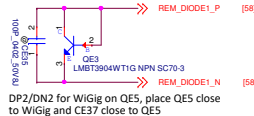
BOARD_ID rise time is measured from 5%~68%.

SYSTEM_ID rise time is measured from 5%~68%.



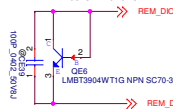
Thermal diode mapping

5085 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	M.2
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

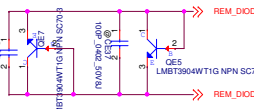
Place under CPU
Place CE35 close to the QE3 as possible

DP2/DN2 for WIGig on QE5, place QE5 close to WIGig and CE37 close to QE5

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.



DN2a/DP2a for DDR on QE7, place QE7 close to DDR and CE46 close to QE7



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Title	MEC5105 support	Rev	0.3
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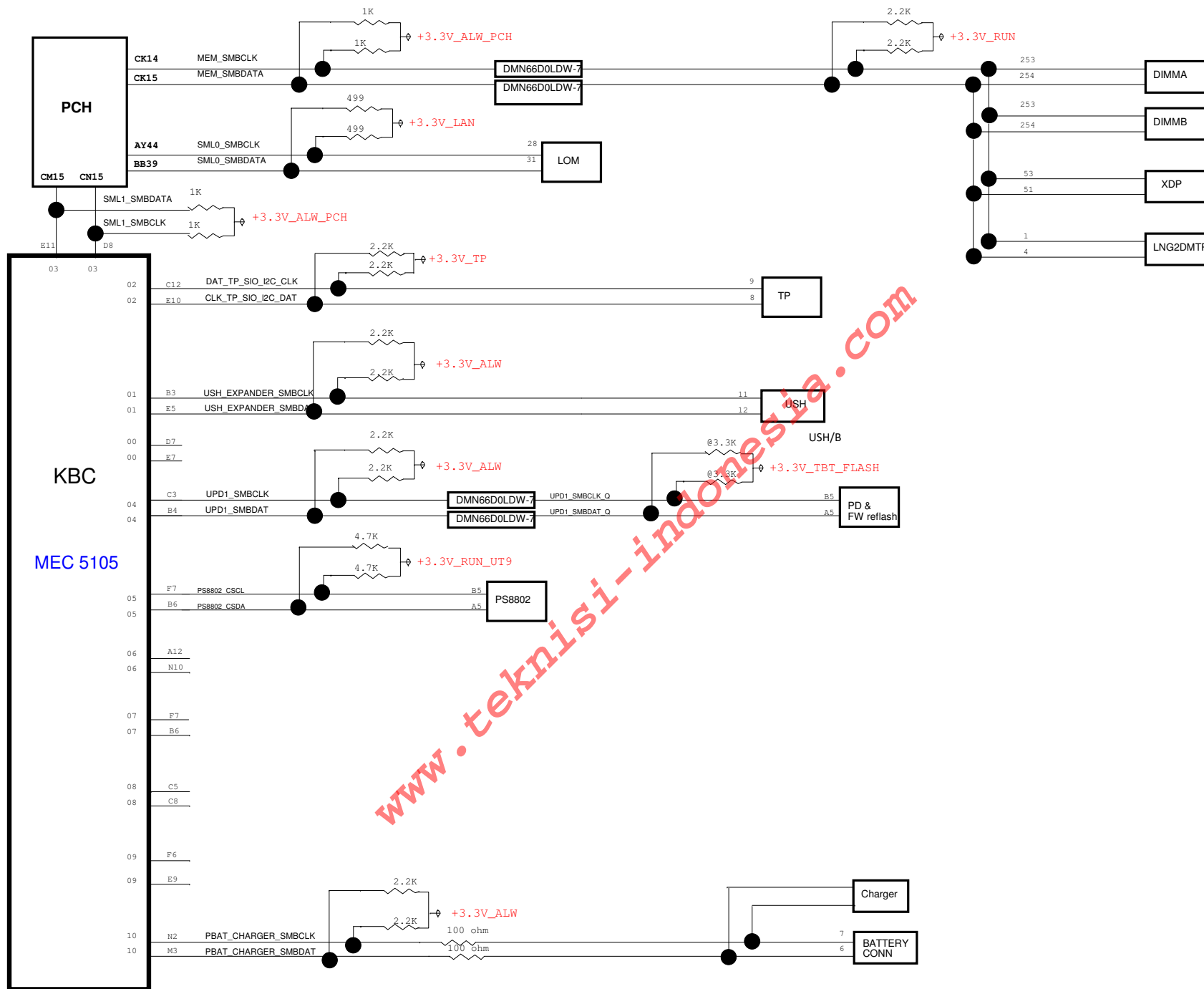
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Compal Electronics, Inc.			
Title			
Secure & Reset IC			
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Reserve

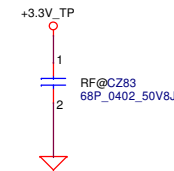
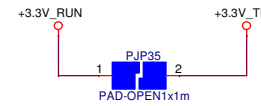
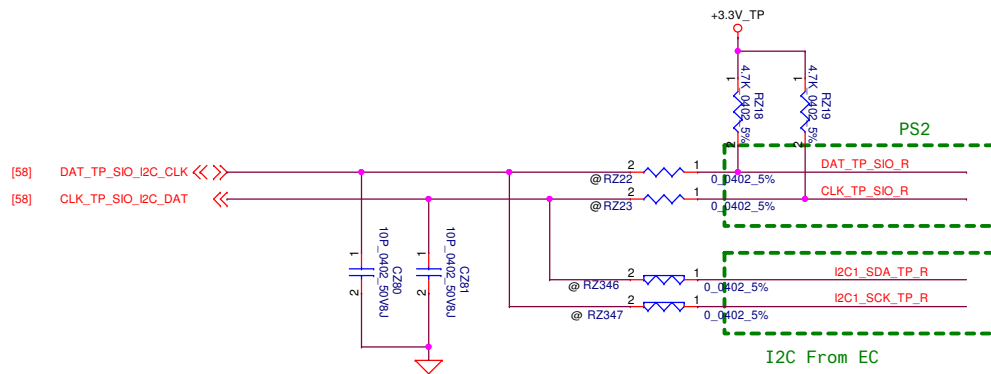
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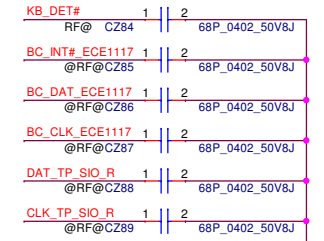


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Title		LED (Controller)	
Size	Document Number	LA-G891P	Rev 0.3
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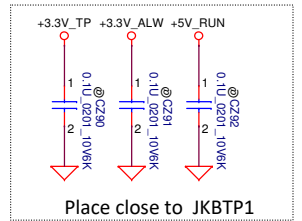
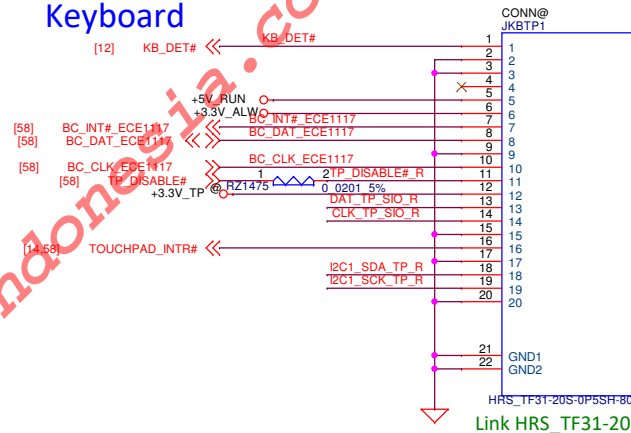
Touch Pad



RF Request



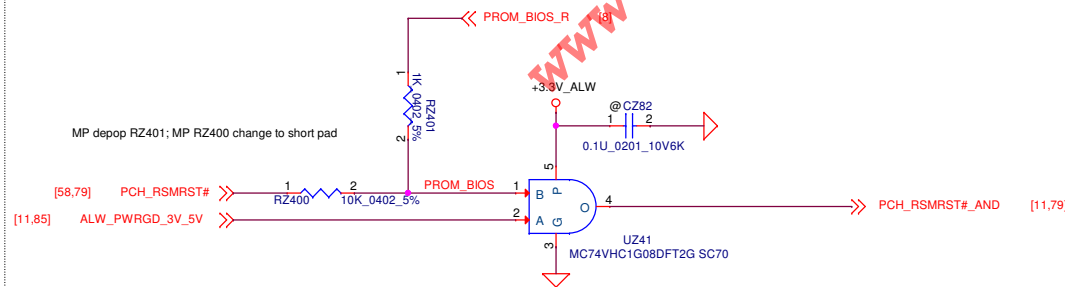
Keyboard



5/29

Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7). For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows. Route PS2 from EC to the touch pad also for contingency plan if I2C has issues.

RSMRST circuit



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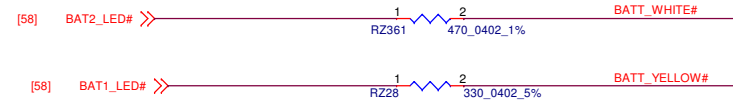
Compal Electronics, Inc.

Keyboard

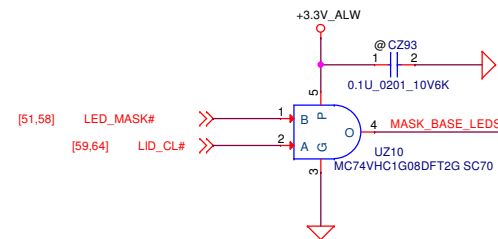
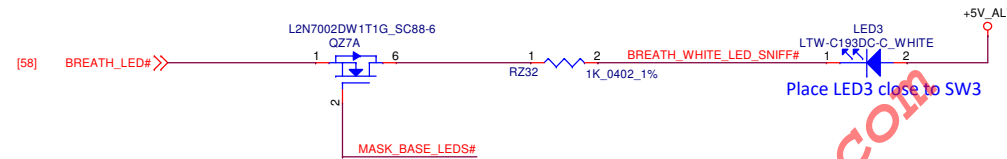
LA-G891P

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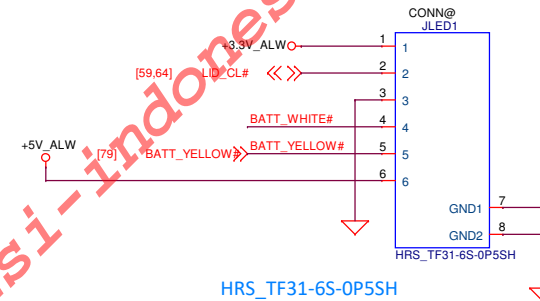
Battery LED



Breath LED



LED board CONN



LED Circuit Control Table

	LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

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Reserve

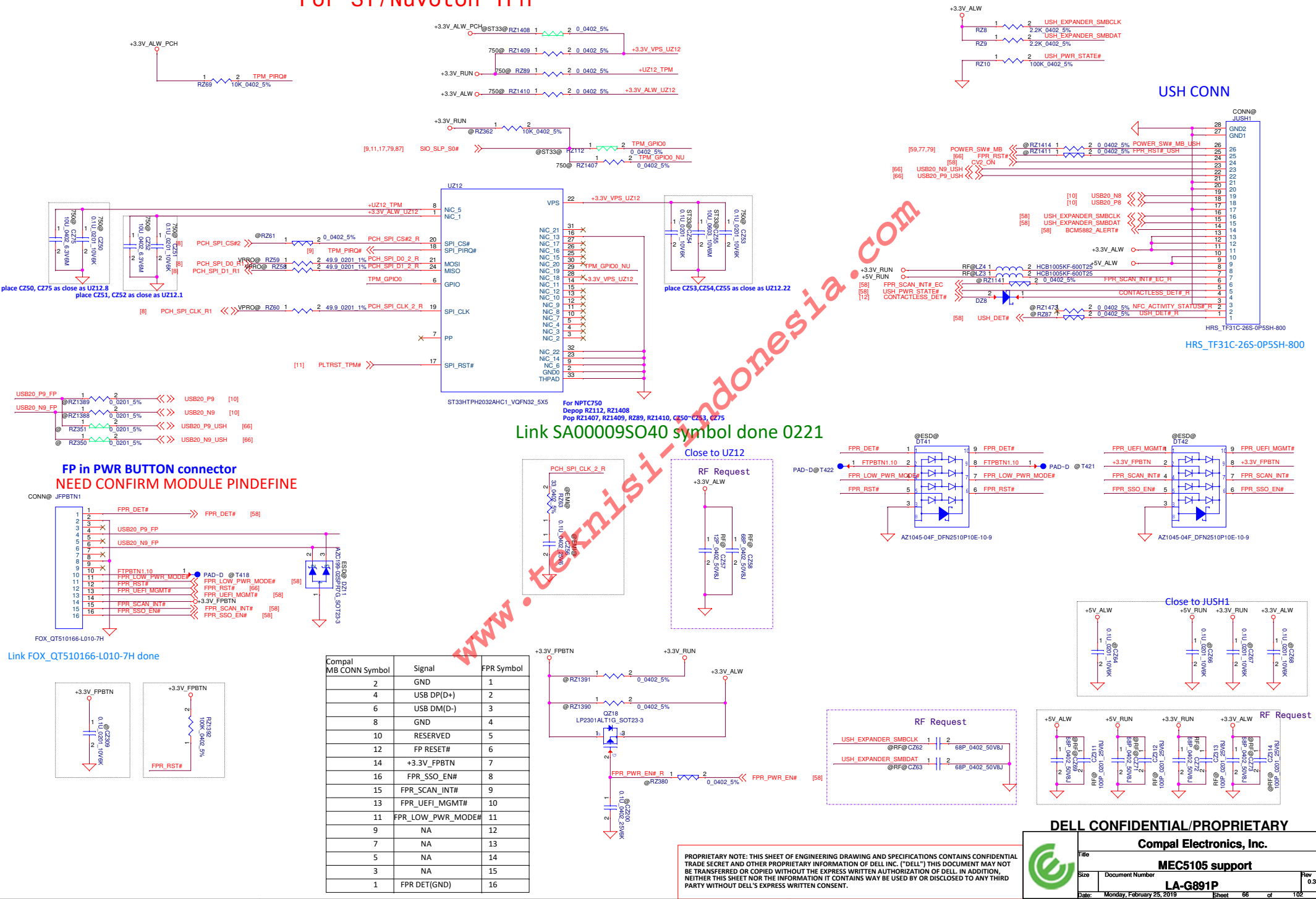
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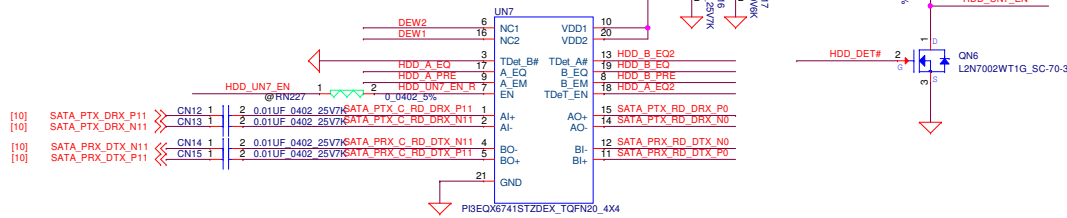
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Title		
KB/TP/LED/LID		
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For ST/Nuvoton TPM



	pin 3	pin 13	pin 16	pin 18
Pericom	TDet_B#	NC	TDet_A#	NC
TI	GND	DEW2	GND	DEW1
Parade	GND	REXT	B_EQ2	DEW
				A_EQ2

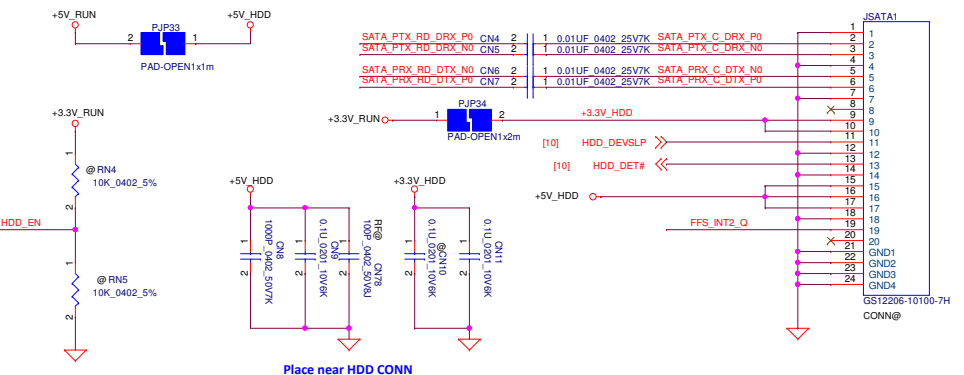
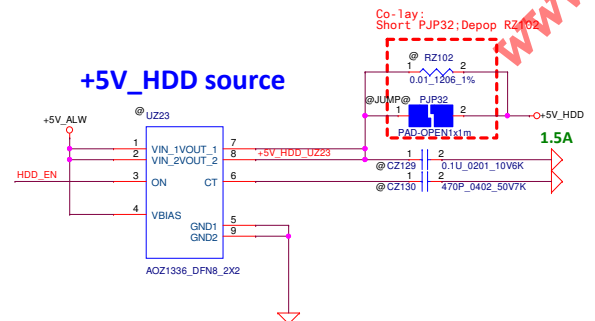
SATA Repeater



	HDD_A_EQ	HDD_B_EQ	HDD_A_EQ2	HDD_B_EQ2	DEW1	DEW2	HDD_A_PRE	HDD_B_PRE
Pericom PI3EQX6741ST	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC	NC	PD (RN7)	PD (RN9)
TI SN75LVCP601	PD (RN11)	NC	PD (RN21)	PD (RN19)	NC (IPU)	NC (IPU)	PH (RN6)	PH (RN8)
Parade PS8527C	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC (1/2 VDD)	PD (RN15)	NC (1/2 VDD)	NC (1/2 VDD)

			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0	3dB	3dB	0	0dB	0dB
		1	6dB	6dB	1	1.5dB	1.5dB
			9dB	9dB			
2nd	TI	0	7dB	7dB	0	0dB	0dB
		1	0dB	0dB	1	-4dB	-4dB
			14dB	14dB		-2dB	-2dB
3rd	Parade	EQ2	EQ1	A_EQ	B_EQ	A_EM	B_EM
		(M = VDD/2)					
		0	M	2.4dB	2.4dB	0	0dB
		0	0	7.4dB	7.4dB	0	0dB
		0	1	14.4dB	14.4dB	0	0dB
		M	M	12.2dB	12.2dB	M	-3.5dB
		M	0	9.4dB	9.4dB	M	-3.5dB
		M	1	13.3dB	13.3dB	M	-1.5dB
		1	M	6.2dB	6.2dB	1	-1.5dB
		1	0	11.2dB	11.2dB	1	-1.5dB
		1	1	5dB	5dB	1	-1.5dB

* red color is current setting



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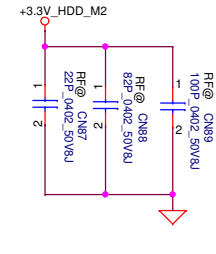
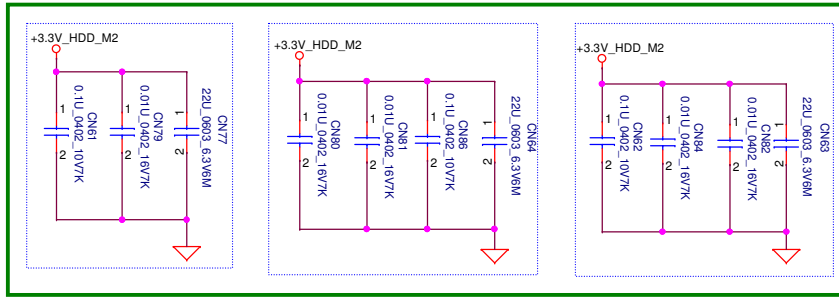
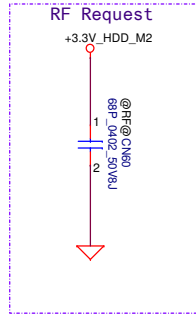
SATA Repeater&HDD CONN

LA-G891P

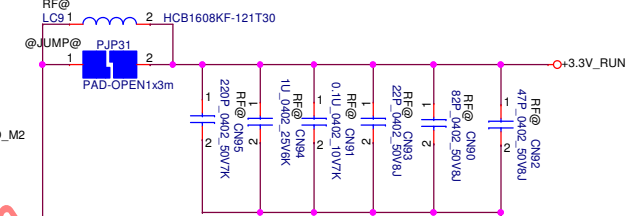
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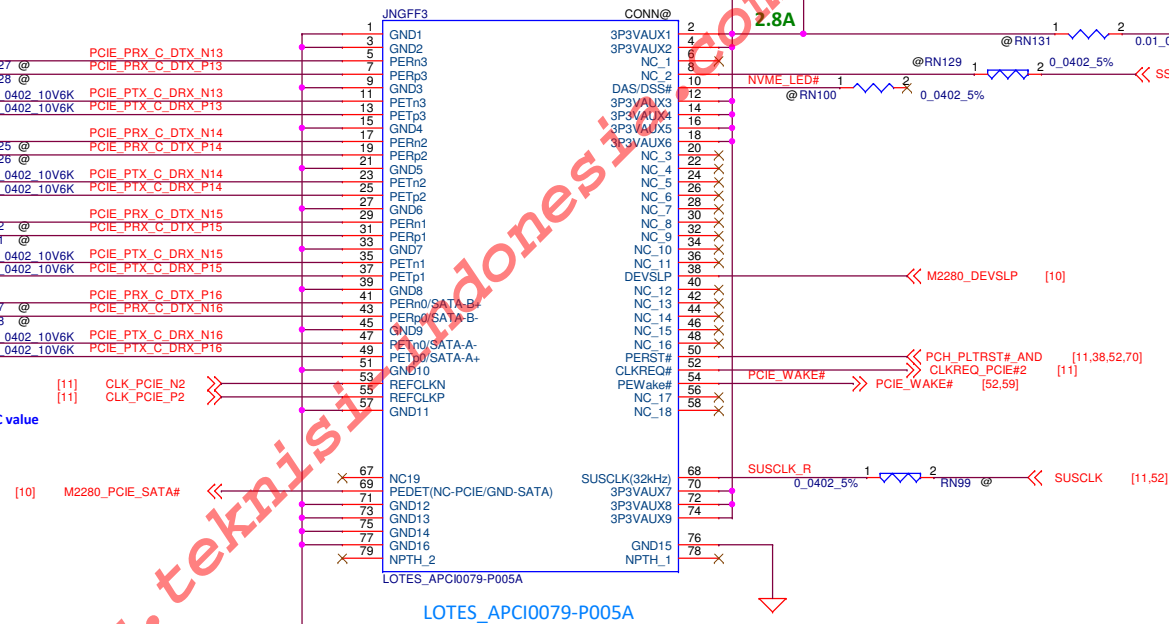
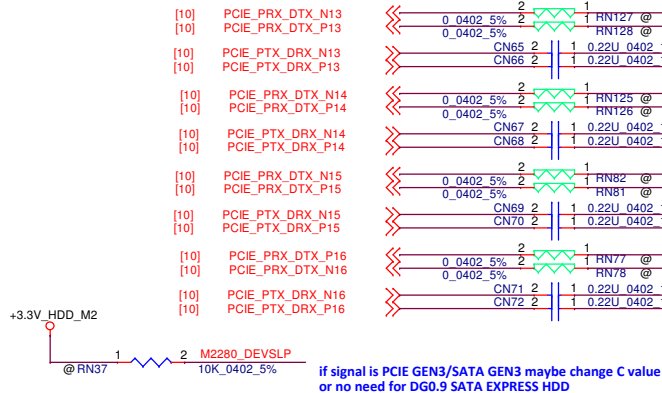
Add Power Decoupling for support Intel Teton Glacier



+3.3V_SSD from SSD storage protection power gate control



2280 SSD
NGFF slot C Key M



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M2 2280 Socket

LA-G891P

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M2 2280 Socket		0.3	
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Size	Document Number		Rev
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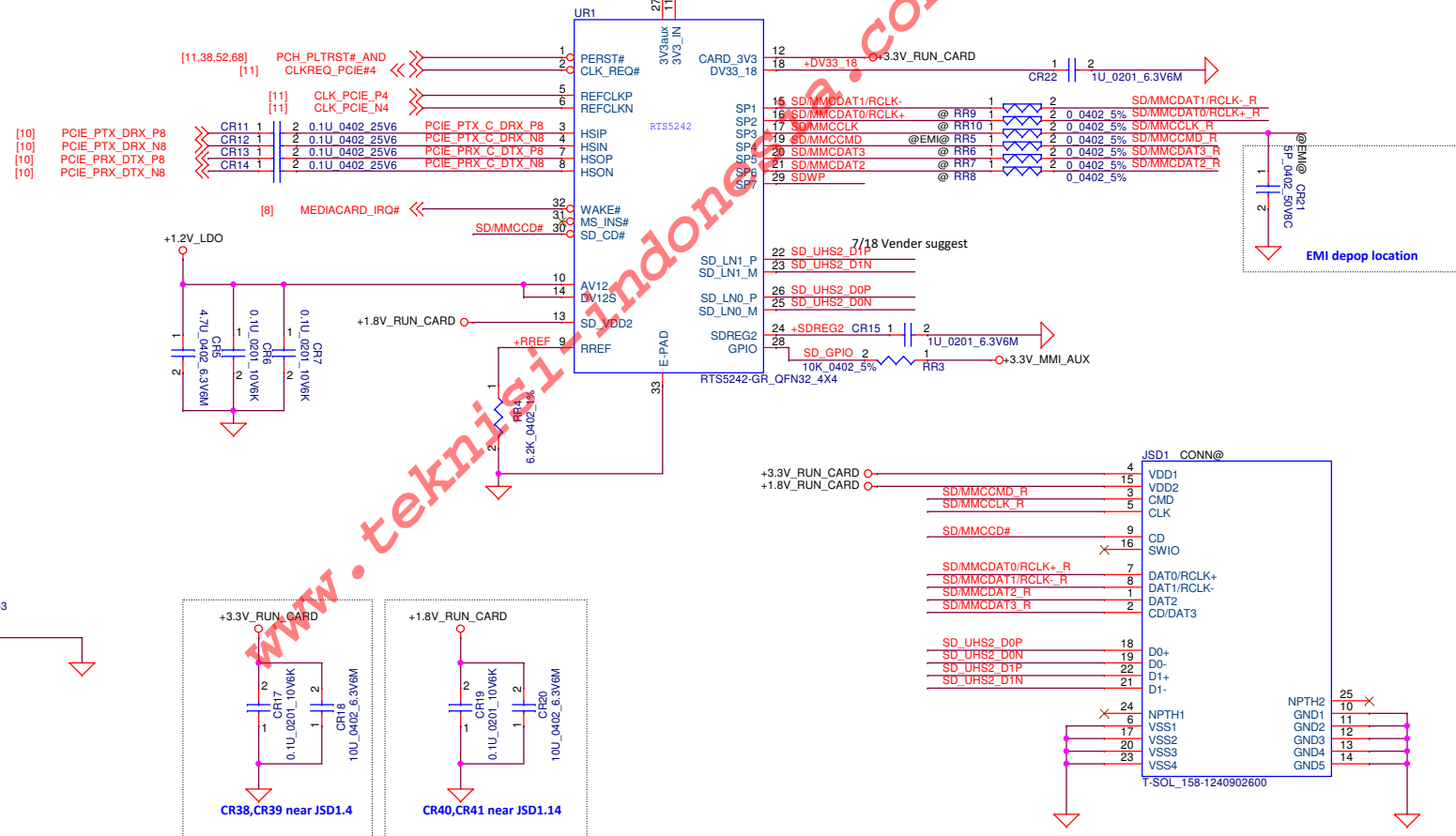
Card Reader RTS5242

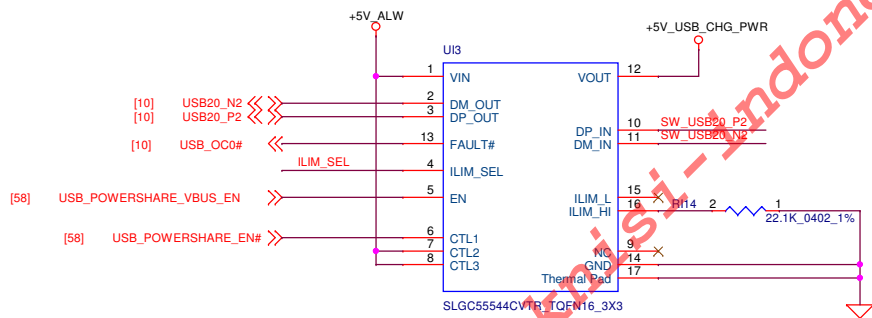
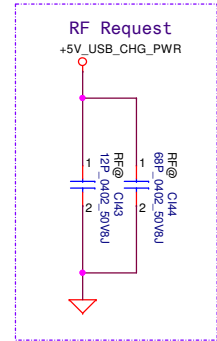
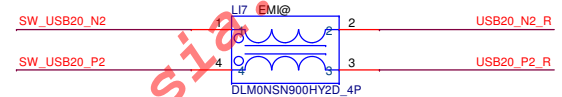
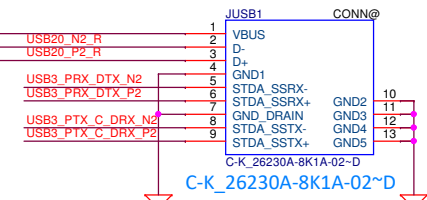
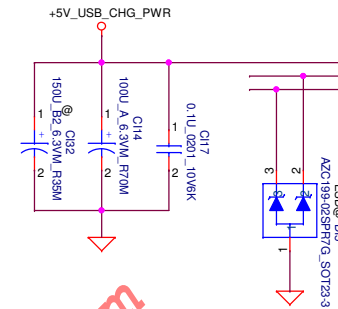
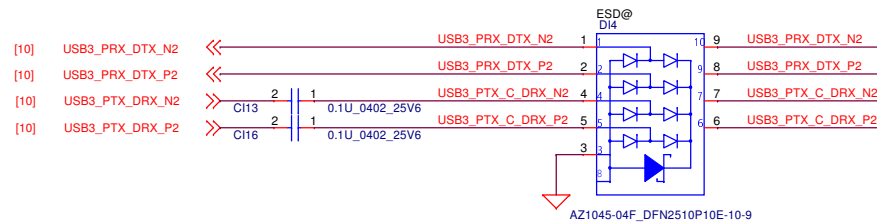
Card Reader RTS5242

LA-G891P

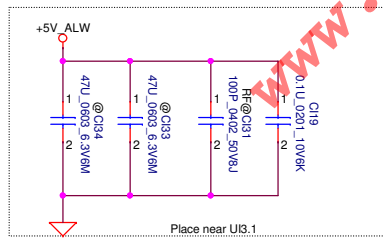
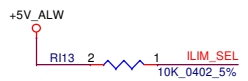
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	LA-G891P	0.3
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MAIN: SLGC55544CVTR



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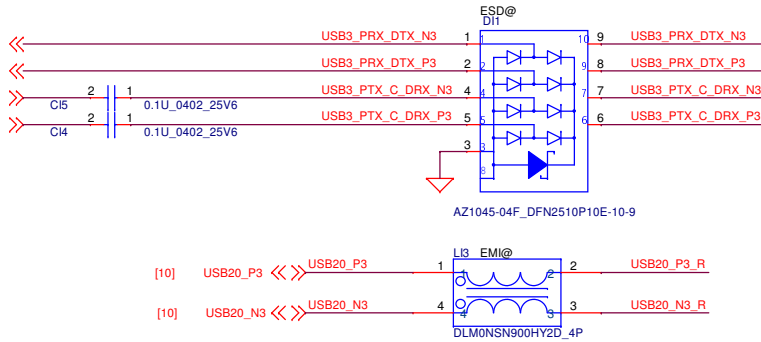
Compal Electronics, Inc.

Title		JUSB1+PS
Size	Document Number	LA-G891P
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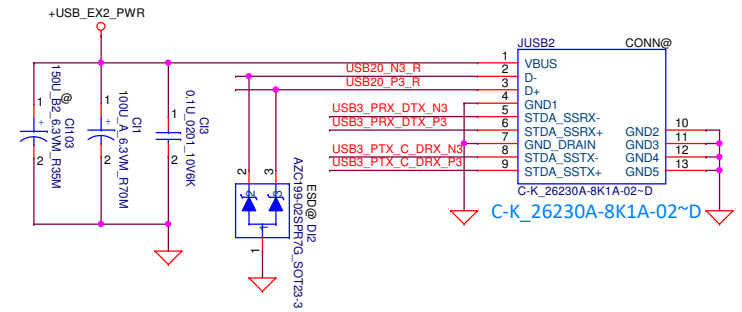
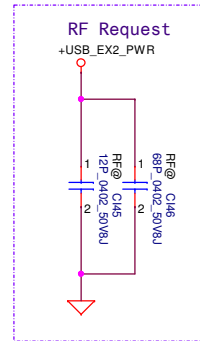
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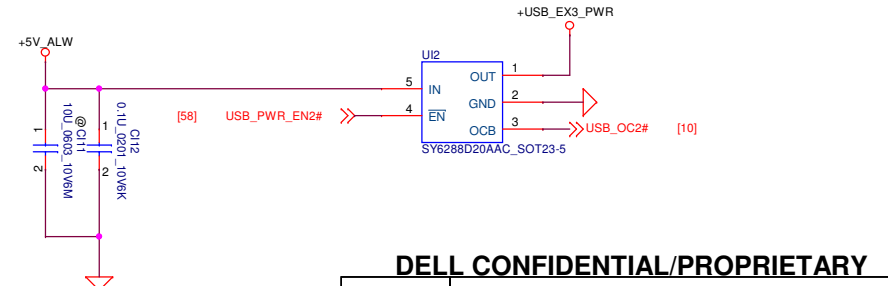
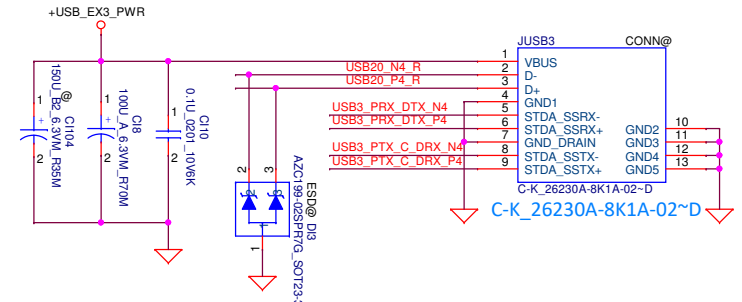
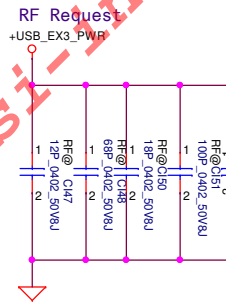
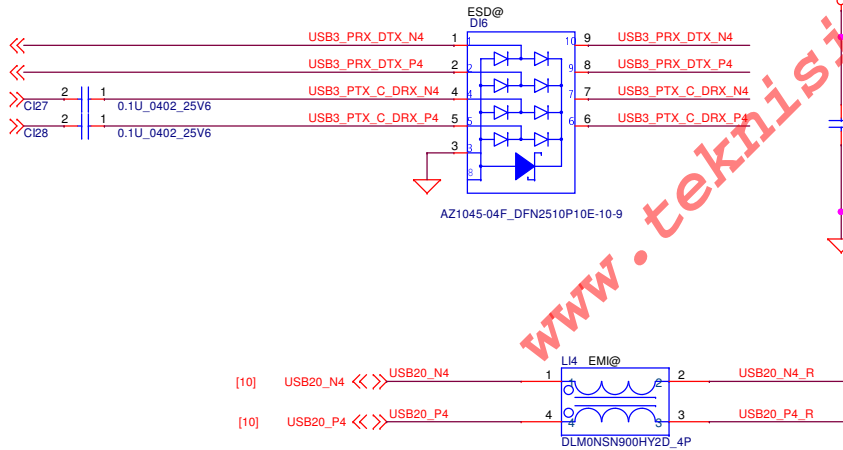
[10] USB3_PRX_DTX_N3
[10] USB3_PRX_DTX_P3
[10] USB3_PTX_DRX_N3
[10] USB3_PTX_DRX_P3



DFB request:
main SM070003Z00 (INPAO_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm



[10] USB3_PRX_DTX_N4
[10] USB3_PRX_DTX_P4
[10] USB3_PTX_DRX_N4
[10] USB3_PTX_DRX_P4



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JUSB2&JUSB3

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Title Dock			
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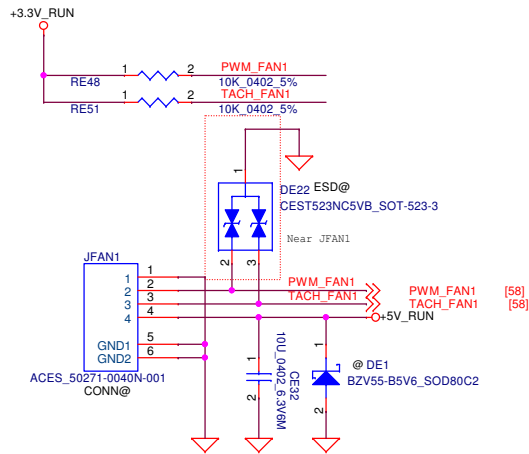
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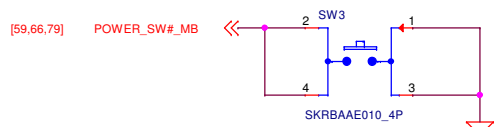
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Title		USB	
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Link 50271-0040N-001 DONE

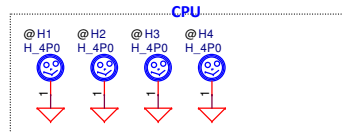
JFAN1 fan follow X9 project PIN DEFINE

POWER & INSTANT ON SWITCH TOP

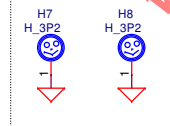


Fiducial Mark

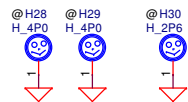
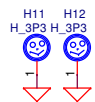
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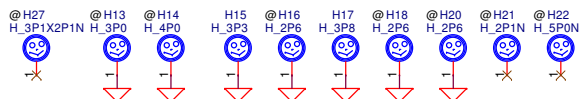
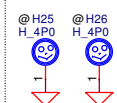
NGFF Standoff



EDP Standoff



FAN Standoff

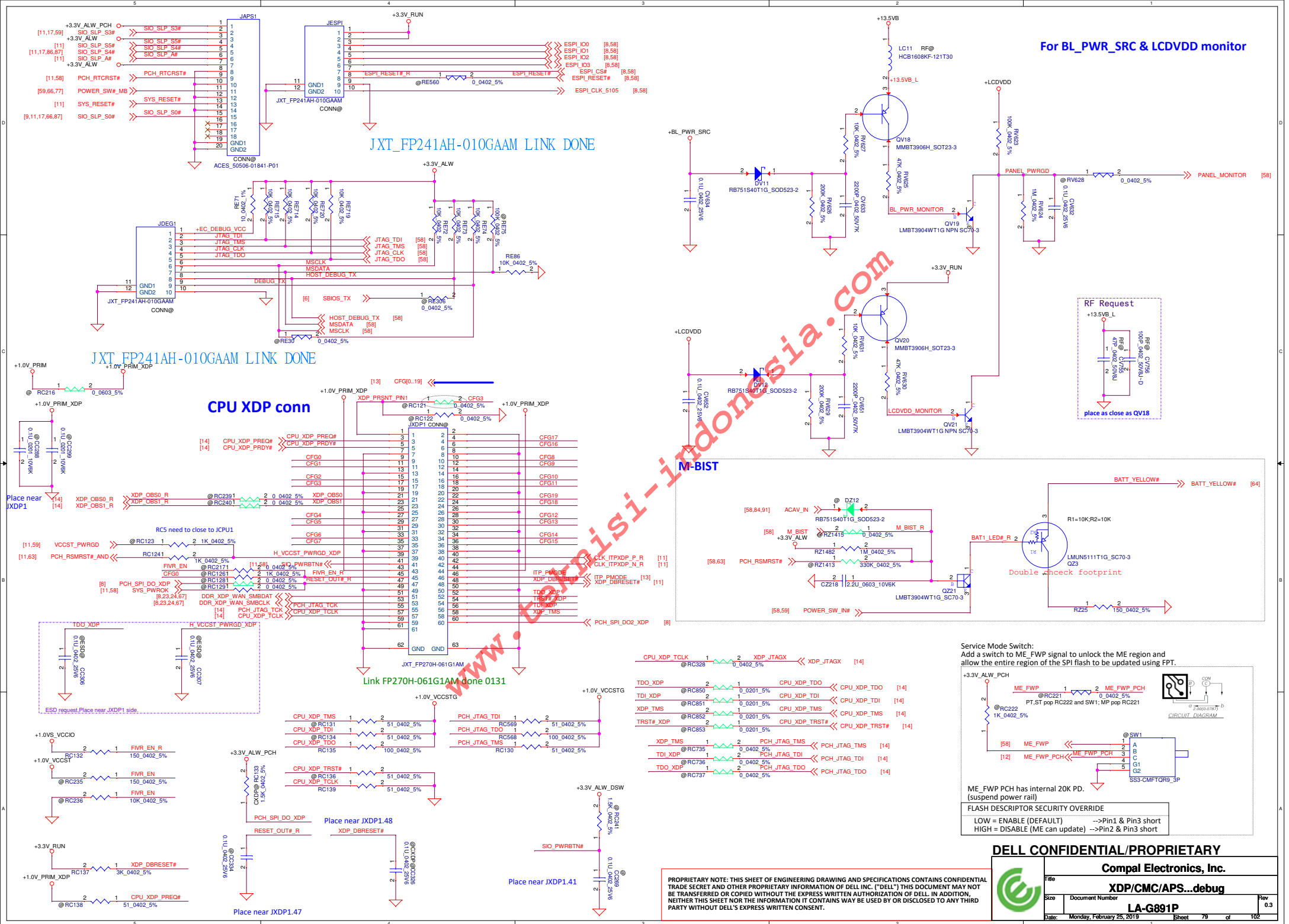


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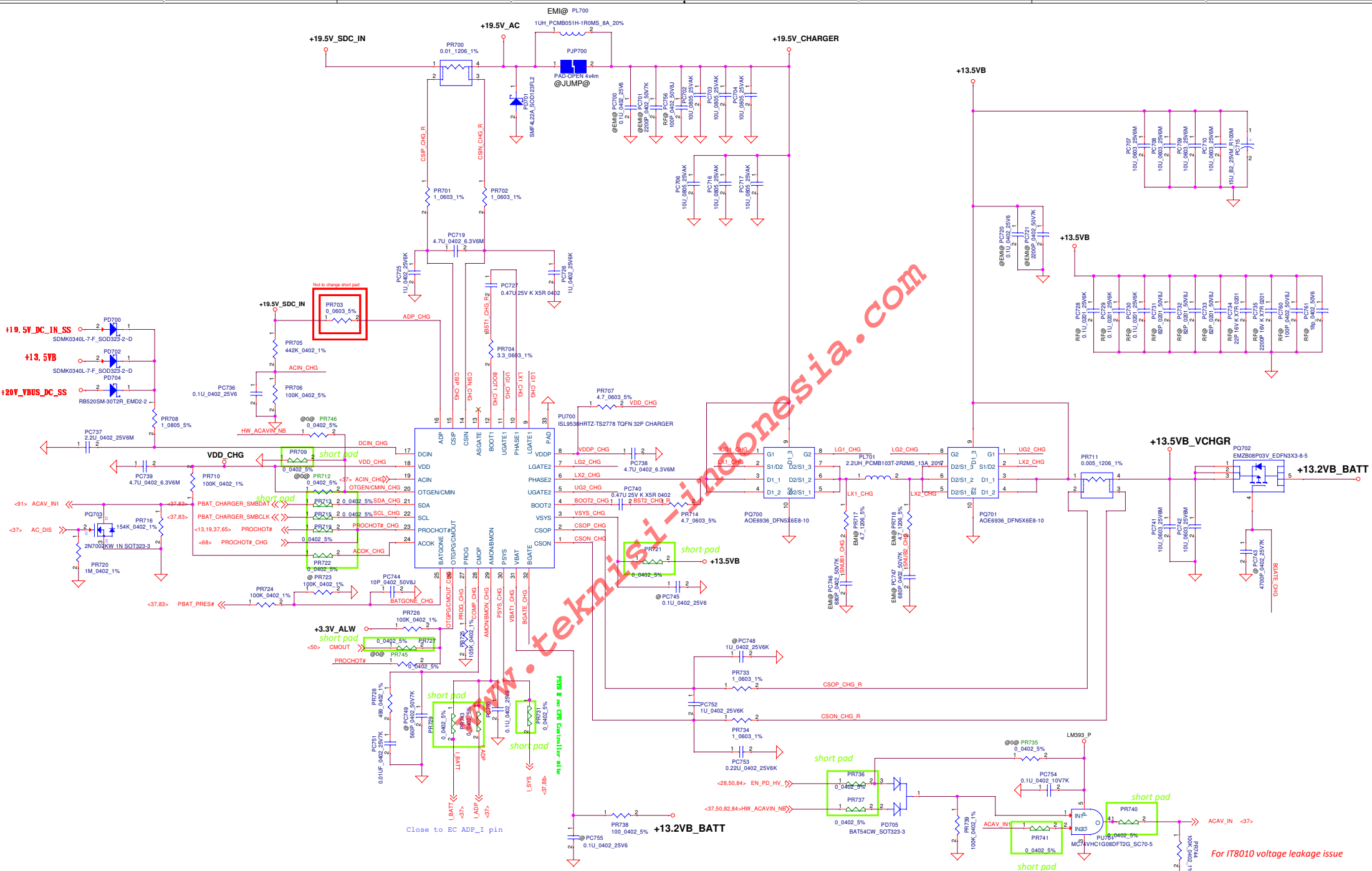
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Compal Electronics, Inc.			
Title	Google Debug		
Size	Document Number	Rev	
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		Compal Electronics, Inc.	
Title		PWR-Block Diagram	
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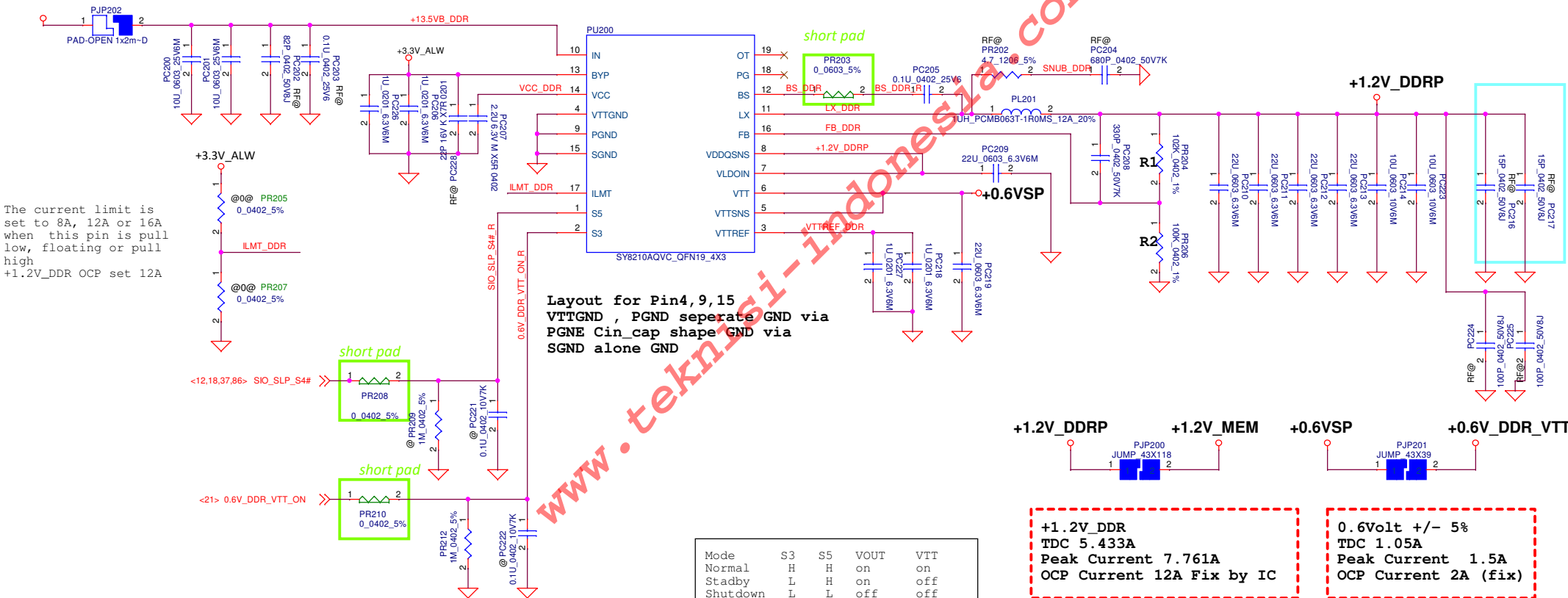


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Compal Electronics, Inc.	
Charger	
LA-891	
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+13.5VB



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Title
+1.2V MEN/+0.6V DDR VTT

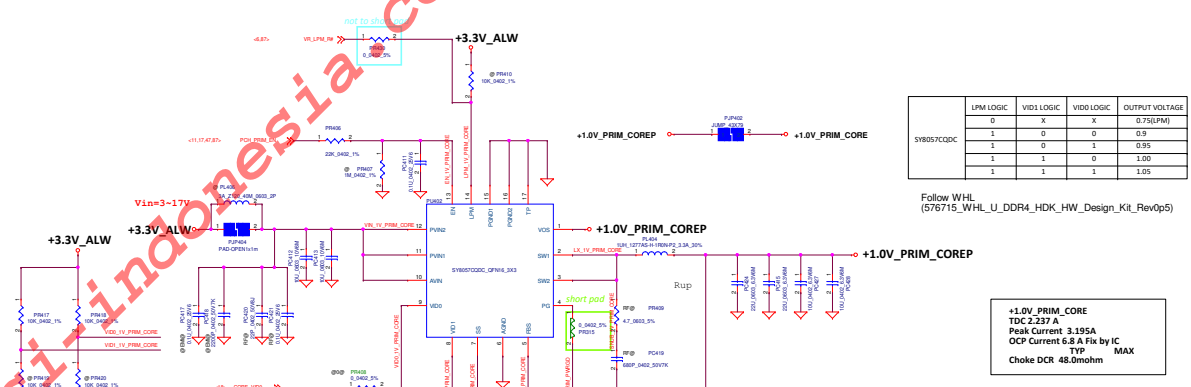
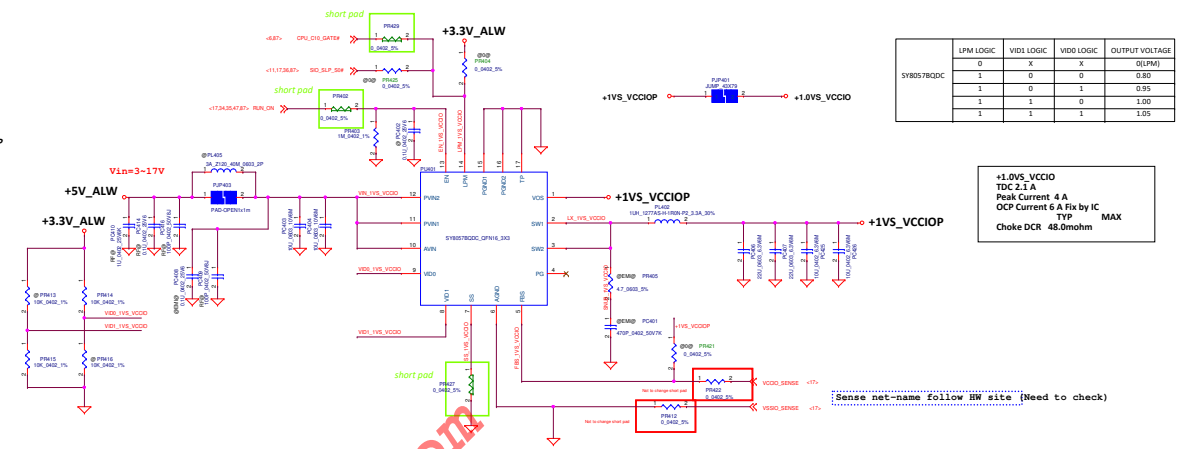
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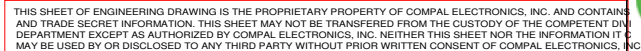
LA-891

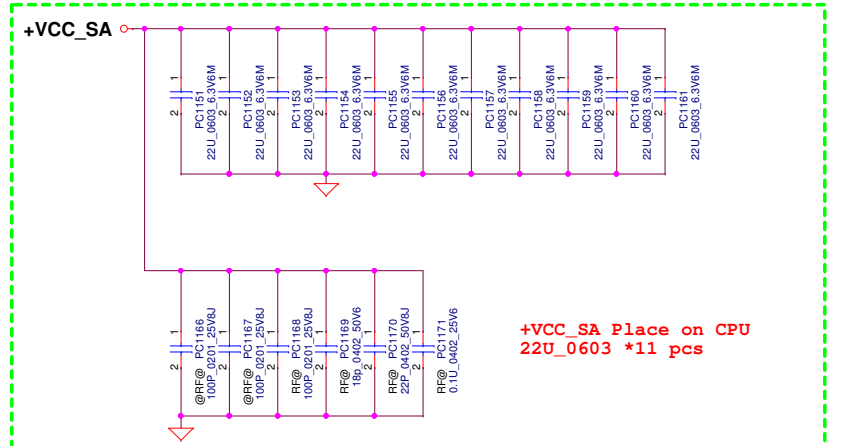
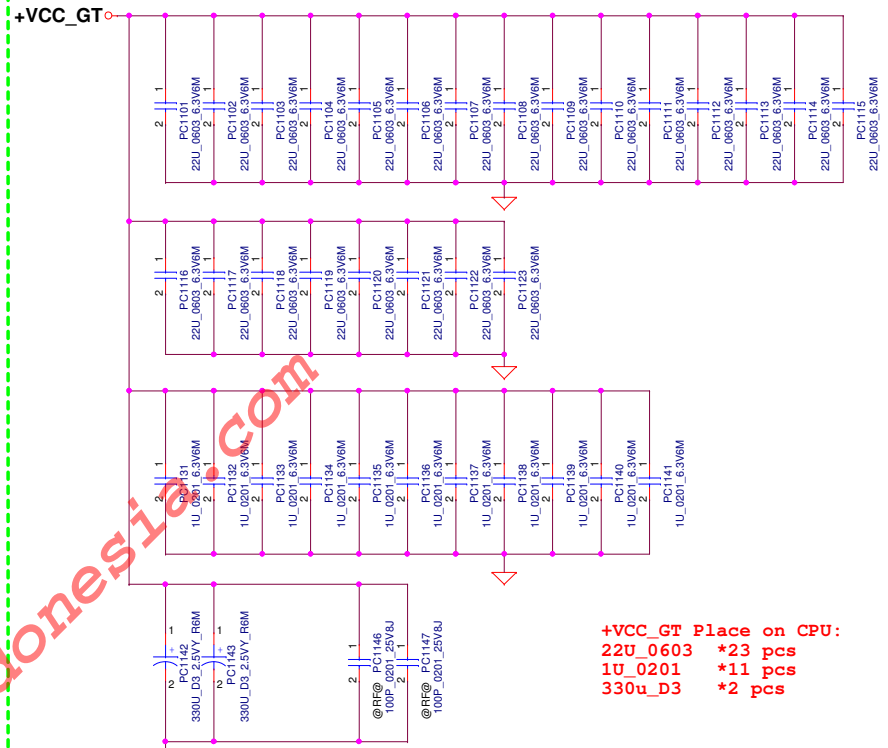
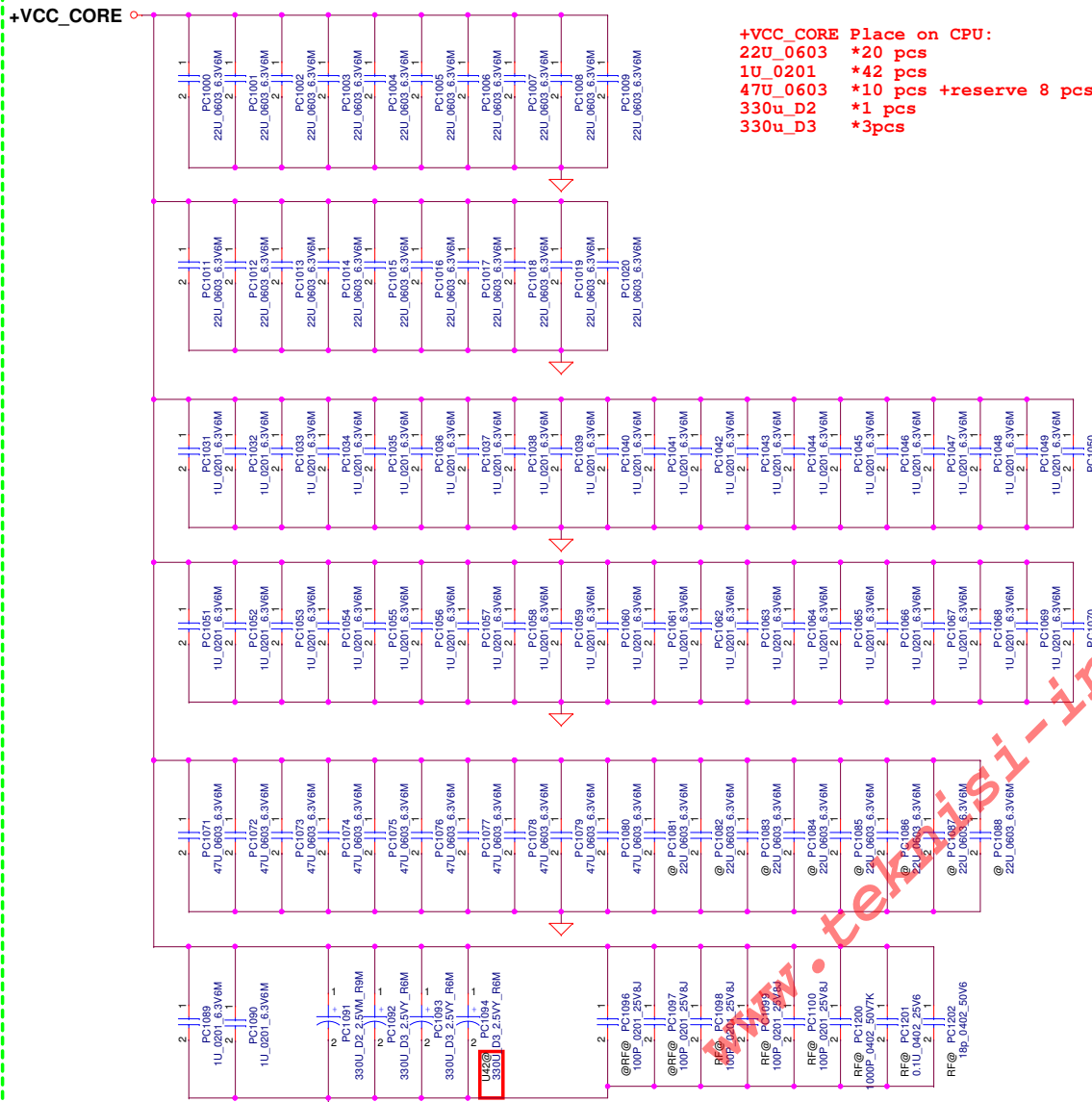
Rev
0.3

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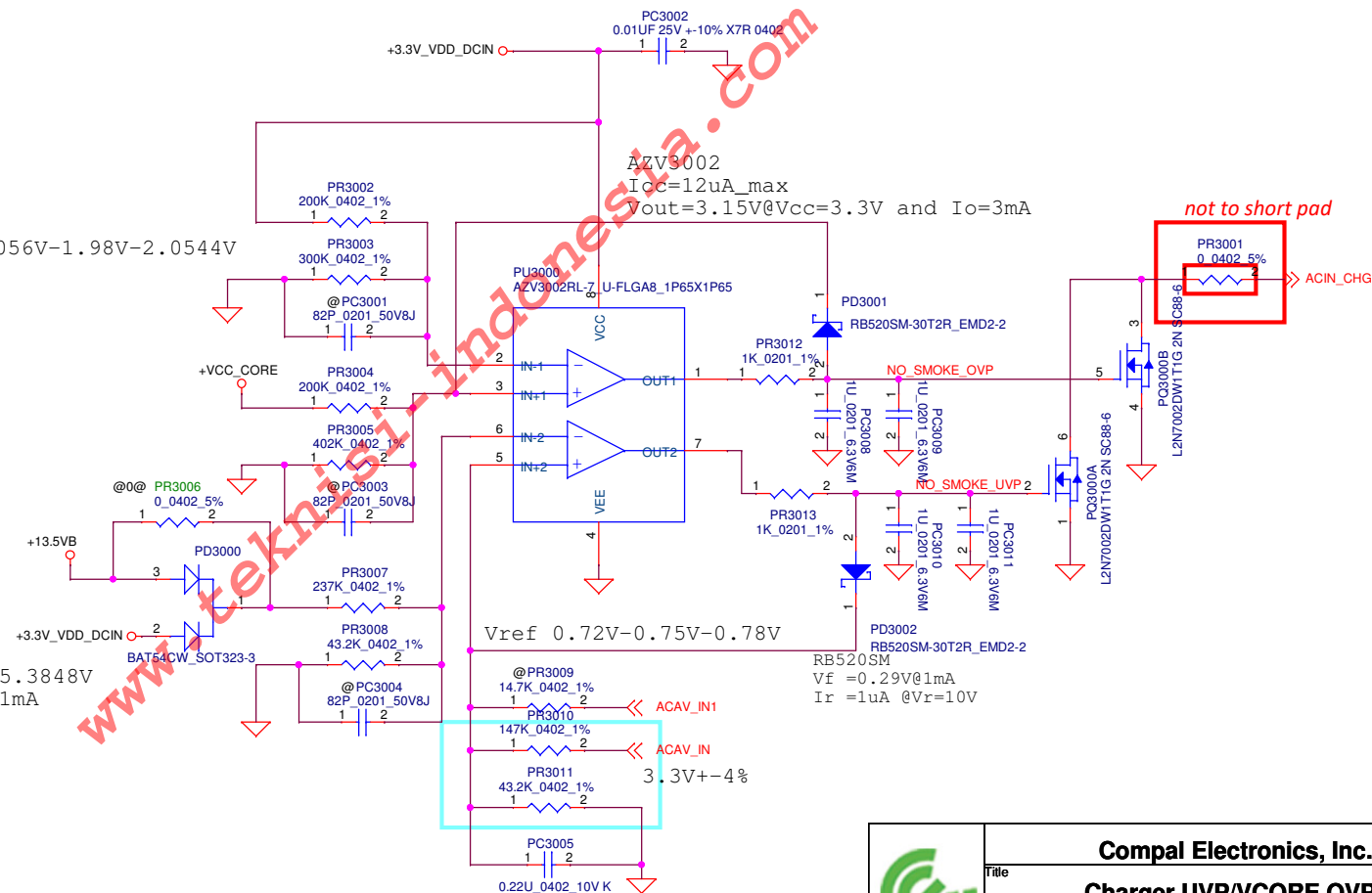
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		Compal Electronics, Inc.	
		CPU Decoupling CAP	
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VIN 4.9952V-5.19V-5.3848V
P3000 Vf = 0.32V @1mA

Vf 1.9056V-1.98V-2.0544V




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	Title			
	Charger UVP/VCORE OVP			
	Size	Document Number		Rev
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Size	Document Number		Rev
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U42


PC626 U42@ 	PR613 U42@ 	PR621 U42@ 	PC624 U42@ 	PC621 U42@ 
0.1U_0402_10%	97.6K_0402_1%	316_0402_1%	0.022U_0402_10%	680P_0402_10%
PR638 U42@ 	PR622 U42@ 	PC616 U42@ 	PC617 U42@ 	
523_0402_1%	2.49K_0402_1%	68P_0402_5%	1200P_0402_10%	

U22

PC626 U22@ 	PR613 U22@ 	PR621 U22@ 	PC624 U22@ 	PC621 U22@ 
0.047U_0402_10%	84.5K_0402_1%	316_0402_1%	0.033U_0402_10%	820P_0402_10%
PR638 U22@ 	PR622 U22@ 	PC616 U22@ 	PC617 U22@ 	
412_0402_1%	1.65K_0402_1%	33P_0402_5%	1200P_0402_10%	

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Version Change List (P. I. R. List)						
Item	Page#	Date	Issue Description	Solution Description	Rev.	
D	1	P089	06/04	Fairchild & AOS Dr.MOS vendor remove PVCC reserved resistor	Delete reserved PR686/PR689/PR681 on PVCC side	X01
	2	P082 P086 P088 P089	06/08 07/02	Change to common PN	1. PC624 change to SE07622K80 (S CER CAP 0.022U 16V K X7R 0402) 2. PC804 change to SE07422K80 (S CER CAP 220P 50V K X7R 0402) 3. PC633 change to SE075472K80 (S CER CAP 4700P 25V K X7R 0402) 4. PL201 change to SH00000YB00 (common P/N) 5. PL614 change to SH00001ED00 (common P/N)	X01
	3	P090	07/12	Merion Top side Z-height limitation	1. Un-stuff PC1094 (U428) 2. Add stuff PC1095 - 330uF (Bottom side)	X01
	4	P088 P099	07/13	CPU tune value by intersil	1. Change the PR636 from 665 Ohm to 634 Ohm. - (VCCSA R1) -> SD00000D280, S RES 1/16W 634 +-1% 0402 2. Change the PR640 from 374 Ohm to 365 Ohm. - (VCCGT R1) -> SD034365080, S RES 1/16W 365 +-1% 0402 3. Change the PC646 from 0.047uF to 0.0022uF. - (VCCGT RC) -> SE075222K80, S CER CAP 2200P 25V K X7R 0402 4. Change the PC642 from 0.033uF to 0.068uF. - (VCCGT RC) -> SE00000J380, S CER CAP 0.068U 16V K X7R 0402 5. Change the PC621 from 680pF to 820pF. - (VCC1A FB RC). -> SE000008980, S CER CAP 820P 25V K X7R 0402 6. Change the PR611 from 1.87kOhm to 9.31kOhm. - (PROG2) -> SD034931180, S RES 1/16W 9.31K +-1% 0402	X01
C	5	P082 P083	07/20	ESD request	PD1, PD2, change to SCA00002A00 for ESD demand	X01
	6	P082	07/30	LPS function test fail on G3 mode. Need to return LDO(PU2) design circuit.	Need stuff item : PU2/ PC10/ PC11/ PR37/ PR3/ PR27/ PR17/ PD800 / PR806 / PR809/ PR832/ PR859 / PR810 / PR813 Need delete location : PR48 / PR34 / PR3 / PR36 / PR37/ PR847 / PR848 / PR849/ PR850 Need un-stuff item : PR851 / PR852 / PR852	X01
	7	P082	07/30	PQ8 gate for non-Backdrive issue	Add R/C delay PR865/PC865 : 100K(SD028100380) and 0.1uF_0402_25V(SE00000G880)	X01
	8	P082	08/10	LM393 resistor value fine tune	PR800 change to 422K_0402_1% (SD034422380) PR815 change to 37.4K_0402_1% (SD034374280) PR832 change to 402K_0402_1% (SD028102380) PR843 change to 82.4K_0402_1% (SD034374280) PR831 change to 1K_0402_1% (SD034100480) PR842 change to 10K_0402_1% (SD034191380)	X01
	9	P088	08/10	ISL95857C solution	PR651 value change to 39.2K for ISL95857C	X01
	10	ALL	08/10	Intel validation tune value by Intersil FAE	Change the PR629 from 90.9kOhm to 86.6kOhm. IMON of GT Change the PR636 from 665 Ohm to 634 Ohm. R1 of SA Change the PR651 from 78.7kOhm to 39.2kOhm. IMON of SA. Change the PR611 from 1.87kOhm to 9.31kOhm. PROG2 Change the PC646 from 2200pF to 6800pF. Cn of GT.	X01
	11	P082 P083	08/15	Follow Schematic naming rule	Re-define the RTC/DCIN/Battery connector from 0 to CONN0.	X01
	12	P082 P083	08/15	Check and modify connector P/N	PJPDC1 - SP02001A500 PBATT1 - SP02001A700 JRTC1 - SP02000R000	X01
	13	P087	08/15	R/C delay fine tune for WHL bring up sequence	1. Modify PR312 / PR406 value from 0 ohm to 22K_0402_1% (SD034220280) 2. PC411 change to stuff 3. Add PC360 : 0.1uF_0402_25V (SE00000G880)	X01
	14	P091	08/20	Remove double pull down resistor	Un-stuff PR505 / PR407	X01
	B	15	P083	08/21	RTC issue	Add RTC detect circuit 1. Add PR9 10Mohm 2. Add PQ13 MOS
16		P091	08/22	Smokeless circuit for Vcore	Add smokeless circuit for Vcore	X01
17		P082	08/22 09/11	LPS function modify	1. Add un-stuff PR870 and pull up source is +20V_VBUS_DC_SS ; 499K_0402_1% (SD034499380) 2. Modify PR831 value to 499K_0402_1% (SD034499380) and pull up source change to +20V_TBTA_VBUS_1 3. Modify PR842 value to 97.6K_0402_1% (SD034976280) 4. PC811 change to SE00000UD00 (10U 6.3V M X5R 0402)	X01
18		P082	08/22	Modify 1 barrel / 1 Type-C External LDO circuit for No Smoke design	1. PD800 change to un-stuff 2. Add PR866 0_0402_5% 3. Add PD803 (BAT54CW_SOT323-3) 4. Add un-stuff PR868 0_0603_5%	X01
A	19	P088 P089	08/22	CPU VR input Low noise MLCC PCB footprint update : C_0603-S3	IA input : PC658 / PC657 / PC656 / PC682 / PC683 / PC684 / PC672 / PC673 GT input : PC675 / PC674 / PC664 / PC665 SA input : PC612 / PC608 IA output : PC1071 / PC1072 / PC1073 / PC1074 / PC1075/ PC1076 / PC1077 / PC1078 / PC1079 / PC1080	X01
	20	P090	08/22	Un-stuffed CPU +VCC_CORE output MLCC change value	Change reserve location from 47uF to 22uF (Keep un-stuff) PC1081 / PC1082 / PC1083 / PC1084 / PC1085 / PC1086 / PC1087 / PC1088	X01
	21	P089	08/22	Remove double net name	Remove PU610 / PU612 / PU613 Dr.MOS pin 15(PVCC) double net name	X01
	22	P087	08/23	Change PU301, PU501 powergood connection netname	Change connection to 1.0V_PRIM_PWRGD from 1.8V_PRIM_PWRGD (PU301, PU501)	X01
23	P087	08/28	R/C for WHL sequence	1. Add PR313 : 100K_0402_5% 2. Add PR314 / PR315 : 0 ohm 3. Reserve PC350 footprint to PG (1.0V_PRIM_PWRGD) signal	X01	
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